DEVELOPMENT OF A PRACTICAL FLEXIBLE SELECTED INTERCONNECTION TECHNIQUE FOR MONOLITHIC CIRCUITS

by

P. R. Malmberg, G. S. Basi, L. J. Koos

Final Report,

June, 1967 to December, 1969

September, 1970

Prepared Under Contract No. NAS 8-20770

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Westinghouse Research Laboratories
Pittsburgh, Pennsylvania 15235

Electronics Research Center
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ABSTRACT

The objective of this program was to develop a practical technique for making custom patterns of interconnections on integrated circuits without the use of masks. The use of a computer-controlled electron beam was proposed for fabricating these interconnections, and this approach was followed throughout. The program has resulted in a fast and accurate method for automatically laying out an interconnection pattern to connect specified subcircuits so as to perform the desired function, and in the means for creating this pattern in metal at the required scale by electron beam lithography without the use of masks or of any photographic processing.

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1.0 INTRODUCTION

In the manufacture of integrated circuits, the ability to change the pattern of the final metal interconnections easily and economically permits use of custom circuits for breadboards and small production runs, using the master slice principle. As it pertains to device and system reliability, a programmed interconnection capability permits the interconnection of a large number of tested subcircuits to form a monolithic subsystem having greatly increased circuit function per external connection or bonding pad. Such a subsystem may be expected to have a significantly lower failure rate than one made of many separate circuit chips because of the relatively large failure rate associated with the greater number of interconnecting leads and wire bonds. Other advantages also accrue from compressing large amounts of circuit function onto a single wafer or chip, such as the short length of circuit interconnections, with reduced capacitance and attendant reduced power per logic function for a given circuit speed.

The aim of the program described in this report was to develop such an interconnection method, using computer-controlled electron beam exposure of electron sensitive resist (electroresist) to delineate conductive paths, thereby eliminating the need for drafting and photographic processes. Previous work at Westinghouse Research on applications of scanning electron microscopes to integrated circuits, and a program already underway under joint Air Force and Westinghouse sponsorship, "Maximum Density Integrated Circuits by Electron Beams", Contract F33615-67-C-1335, provided a sound basis for the present program.

The effort to be described was directed principally at refining the computer-controlled electron beam exposure apparatus and related software, developing software to provide custom interconnection geometries, developing a two-stage single level metallization process, and developing an adequate registration method for successive electron beam-produced patterns.

The test vehicle adopted for the program was a 1-bit adder, made from a redundant array of gates. Viable gates, as determined by probe test, were to be interconnected to form the adder. Originally, only the final, custom, metal interconnection was to be defined by electron beam writing on electroresist, and the other device patterns by conventional photolithographic procedures. During the program, however, it became evident that a distortion of about 0.5% existing in the electron beam pattern would make registration impossible to achieve between optical and electron beam patterns.

To overcome this difficulty, all patterns required both for device fabrication and for final metallization were made by the electron beam method.

2.0 1-BIT ADDER TEST VEHICLE

The choice of vehicle to demonstrate the flexible, selected interconnection technique had to be a compromise between subsystems so small that the relatively unsophisticated interconnection program would fail to have sufficient generality, and subsystems so large that the extended computer programming required would make little further contribution to the demonstration.

A one-bit adder, requiring about 10 to 15 NAND gates, was chosen as representing a suitable compromise between these extremes. This vehicle serves to illustrate all the essential factors involved in maskless discretionary interconnection of viable gates, and represents a useful subsystem of wide application to present-day systems.

2.1 LOGIC SELECTION

The 1-bit adder logic function is described by the following table:

Input			Output	
Previous Carry C	Summand A	Summand B	Sum S	Carry C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1-Bit Adder Logic Function

Table 2.1

This function may be realized by many different but logically equivalent circuit configurations that have relative advantages and disadvantages with regard to speed, complexity, and power dissipation. These may be divided into two classes, namely (1) those using serial addition of the three inputs, two at a time, and (2) those using parallel addition of the three inputs. A review of the various possibilities narrowed the selection to the two adders shown in Figs. 2.1 and 2.2.

The 11-gate adder in Fig. 2.1, which is of the parallel variety, has a logic function which may be represented by

$$S_n = An \cdot B_n' \cdot C_{n-1} + (A_n + B_n + C_{n-1}') \cdot \overline{(A_n \cdot B_n + A_n' \cdot C_{n-1} + B_n' \cdot C_{n-1})},$$

and $C_n = A_n' \cdot B_n + A_n' \cdot C_{n-1} + B_n' \cdot C_{n-1}$,

where . means AND, + means OR, and $\overline{}$ means NOT.

Fig. 2.2 shows a 10-gate adder of the serial variety with a logic function given by

$$S_n = (\overline{A_n'} \cdot B_n + A_n' \cdot \overline{B_n}) \cdot \overline{C_{n-1}} + \overline{(\overline{A_n} \cdot B_n + A_n' \cdot \overline{B_n})'} \cdot C_{n-1}$$

$$= \overline{A_n'} \cdot B_n \cdot \overline{C_{n-1}} + A_n' \cdot \overline{B_n} \cdot \overline{C_{n-1}} + \overline{A_n'} \cdot \overline{B_n'} \cdot C_{n-1} + A_n' \cdot B_n' \cdot C_{n-1}, \text{ and}$$

$$C_n = A_n' \cdot B_n + (A_n' \cdot \overline{B_n} + \overline{A_n'} \cdot B_n) \cdot C_{n-1}$$

$$= A_n \cdot B_n' \cdot C_{n-1} + A_n' \cdot B_n' \cdot \overline{C_{n-1}} - A_n' \cdot \overline{B_n} \cdot C_{n-1} + \overline{A_n'} \cdot B_n' \cdot C_{n-1}$$

$$= A_n' \cdot B_n + A_n' \cdot C_{n-1} + B_n' \cdot C_{n-1}.$$

Both inputs and outputs for this version must be in complementary form, or, what is equivalent, must use negative logic.

A comparison of the gate requirements and power/speed characteristics of these two configurations is shown in Table 2.2. Although the adder of Fig. 2.1 has a faster carry, it requires a larger range of

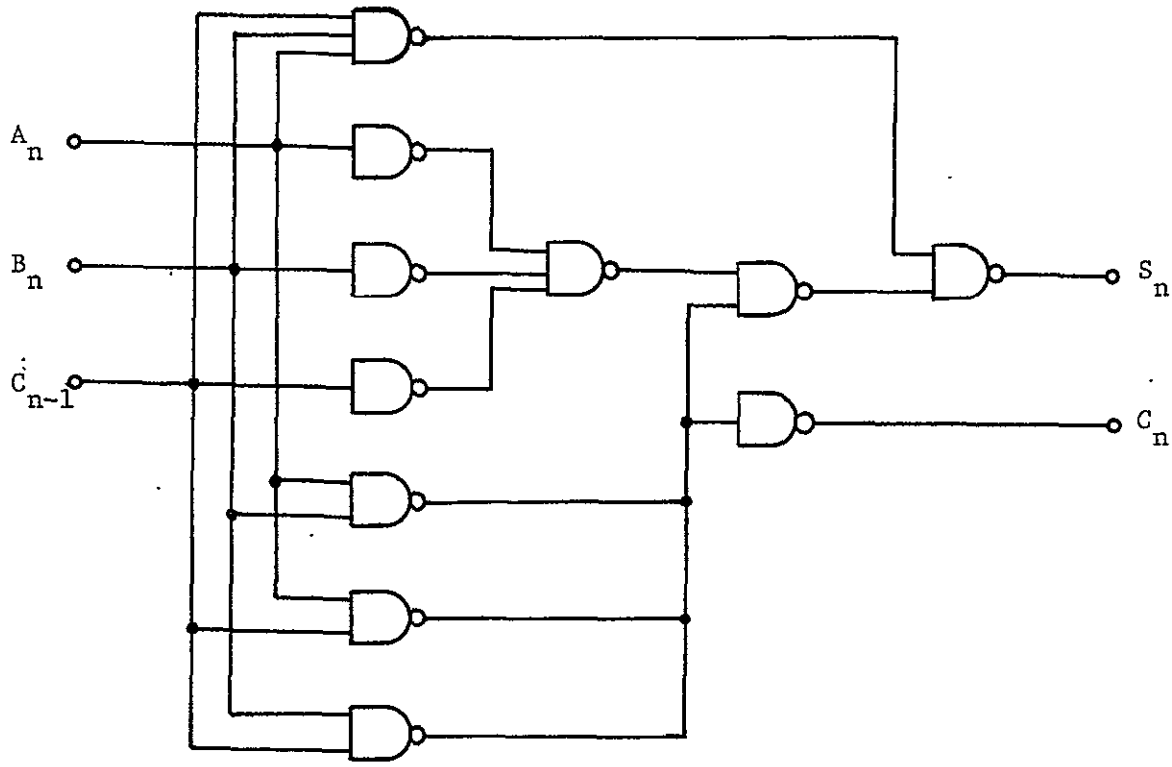


Fig. 2.1 1-bit adder, parallel logic

Dwg. 859A328

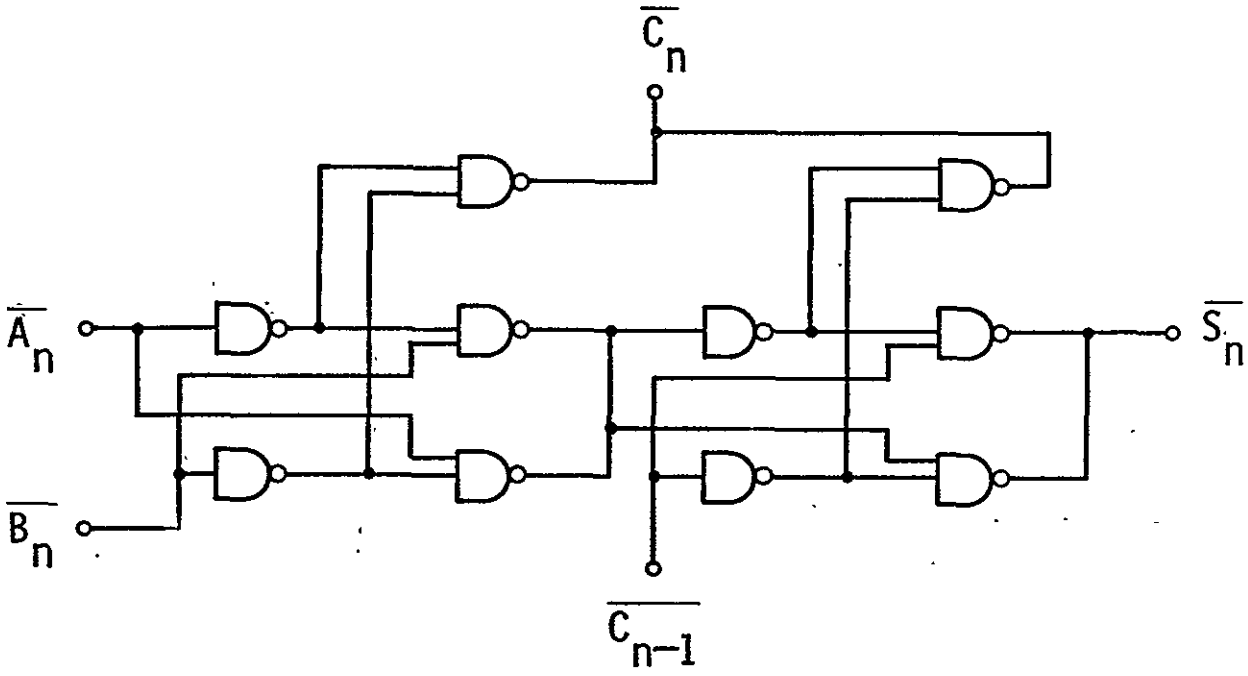


Fig. 2.2 1-bit adder, serial logic

fan-in and fan-out for its constituent gates than that of Fig. 2.2. The sum delay is the same for both circuits. Table 2.2 also shows that the 10-gate version requires 20% fewer gate inputs. In view of this study and comparison, the 10-gate adder, using a 2-in, 4-out gate and working with negative IN/OUT logic levels was selected as best suited for the program vehicle.

	Gate Complement			Total Gates, Type	Total Gate Inputs	Gates On, Max/Min	Sum Delay**	Carry Delay**
	No.	Fan-In	Fan-Out*					
Fig. 2.1 Parallel Logic	4	1	1	11: 3 In, 6 Out	20	7/3	4T	3T
	2	2	2					
	2	3	1					
	3	2	6					
Fig. 2.2 Serial Logic	2	1	1	10: 2 In, 4 Out	16	6/3	4T	4T
	2	1	2					
	4	2	3					
	2	2	4					

*Collector Load Counted as 2 Loads

**T = Average Delay Per Gate

Comparison of 1-Bit Adder Characteristics

Table 2.2

In order to confirm the results of this study a breadboard model of the 10-gate adder was constructed from DTL gates, using 2-1/2 Westinghouse WC-266D packages of quad 2-input NAND gates. The operation of the breadboard version satisfied the adder truth table, and the measured operating speeds substantiated the estimates for maximum sum and carry delays of 4T, where T is the propagation time per gate. Table 2.3 shows the observed delay times for various input transitions.

Initial			Final			Output Delay, μS		Notes
A_1	B_1	C_o	A_1	B_1	C_o	S_1	C_1	
0	0	0	1	1	1	.04	.04	Input Step .01 μS Rise & Fall Time
1	1	1	0	0	0	.05	.05	Operating Time Per Gate, T, $\cong$ .02 μS
0	0	0	0	0	1	.04	--	
0	0	1	0	0	0	.05	--	
0	0	0	1	0	0	.08	--	Same result for B_1 only
1	0	0	0	0	0	.08	--	
0	0	0	1	1	0	--	.04	
1	1	0	0	0	0	--	.05	
0	0	0	1	0	1	--	.08	Same result for B_1 & C_o
1	0	1	0	0	0	--	.05	

Operating Delays for 10-Gate Adder Made From (W) WC-266D DTL Integrated Circuits

Table 2.3

2.2 GATE DESIGN

The logic gate for use in the 1-bit adder was chosen from considerations of low complexity, relatively fast speed, conventional logic levels, conventional processing (up to the final metal), and moderate power requirements. The choice was a basic transistor-transistor logic, T^2L, without output drive transistors, the circuit of which is shown in Fig. 2.3. Several additional leads spanning the supply buses and output connections by means of diffused undercrossings are included to permit final logic interconnection at one level without external crossovers. The use of this gate with small area requirements but with reduced drive capability is especially suitable for LSI applications where most outputs terminate on the wafer, and where buffer amplifiers or drivers may be used where necessary to communicate with the rest of the system external to the wafer. The resistor values chosen for this gate, as shown in Fig. 2.3, give a dissipation per gate, at V_{cc} = 6 volts, of 12 mW ON, 3 mW OFF. In a 10-gate adder array, this design would dissipate a total of 84 mW maximum, 57 mW minimum, apart from dissipation of the unused, redundant gates. The latter can be permanently connected in the OFF condition, restricting their dissipation to 3 mW each. The initial layout for this gate is shown in Fig. 2.4. It measured 300 μ x 350 μ overall, and was designed for use in a 4 x 6 gate array. Anticipated speed for this gate was 10 to 15 nS. The capacitance of interconnecting logic leads, which are 5 μ wide, is about 1.5×10^{-16} Fd per micron length. A typical logic lead on the adder has a length of about 1000 μ, giving an average lead capacitance of 1.5×10^{-13} Fd. The

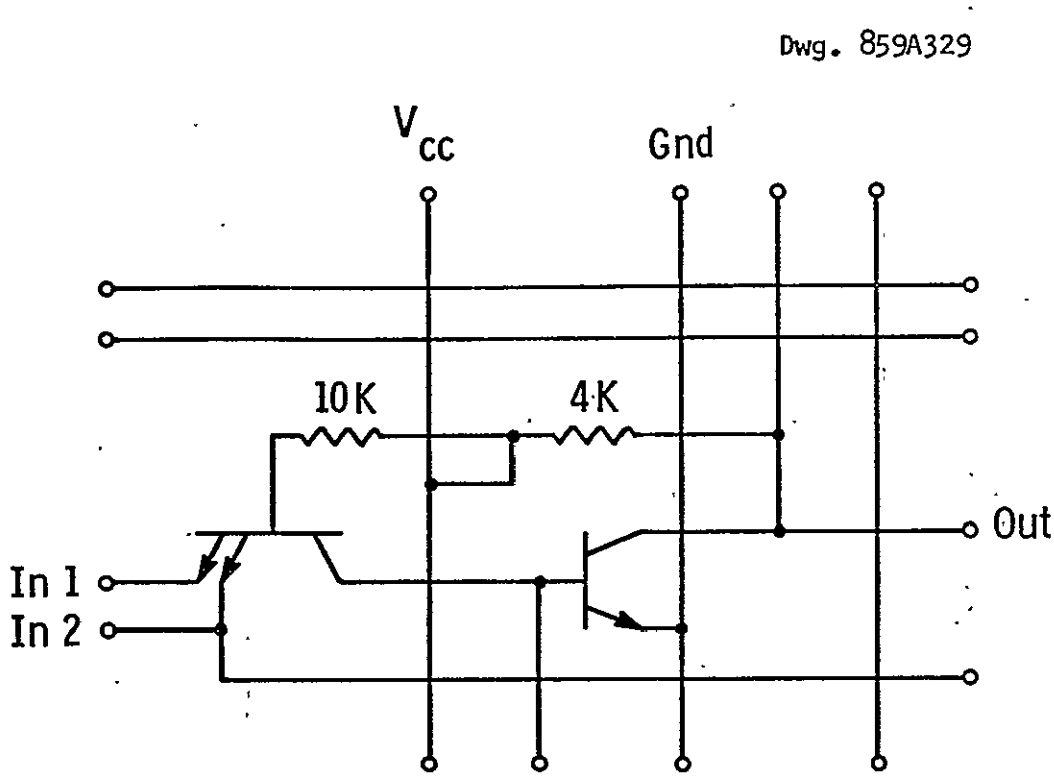


Fig. 2.3 T^2L NAND gate for 1-bit adder

Dwg. 859A330

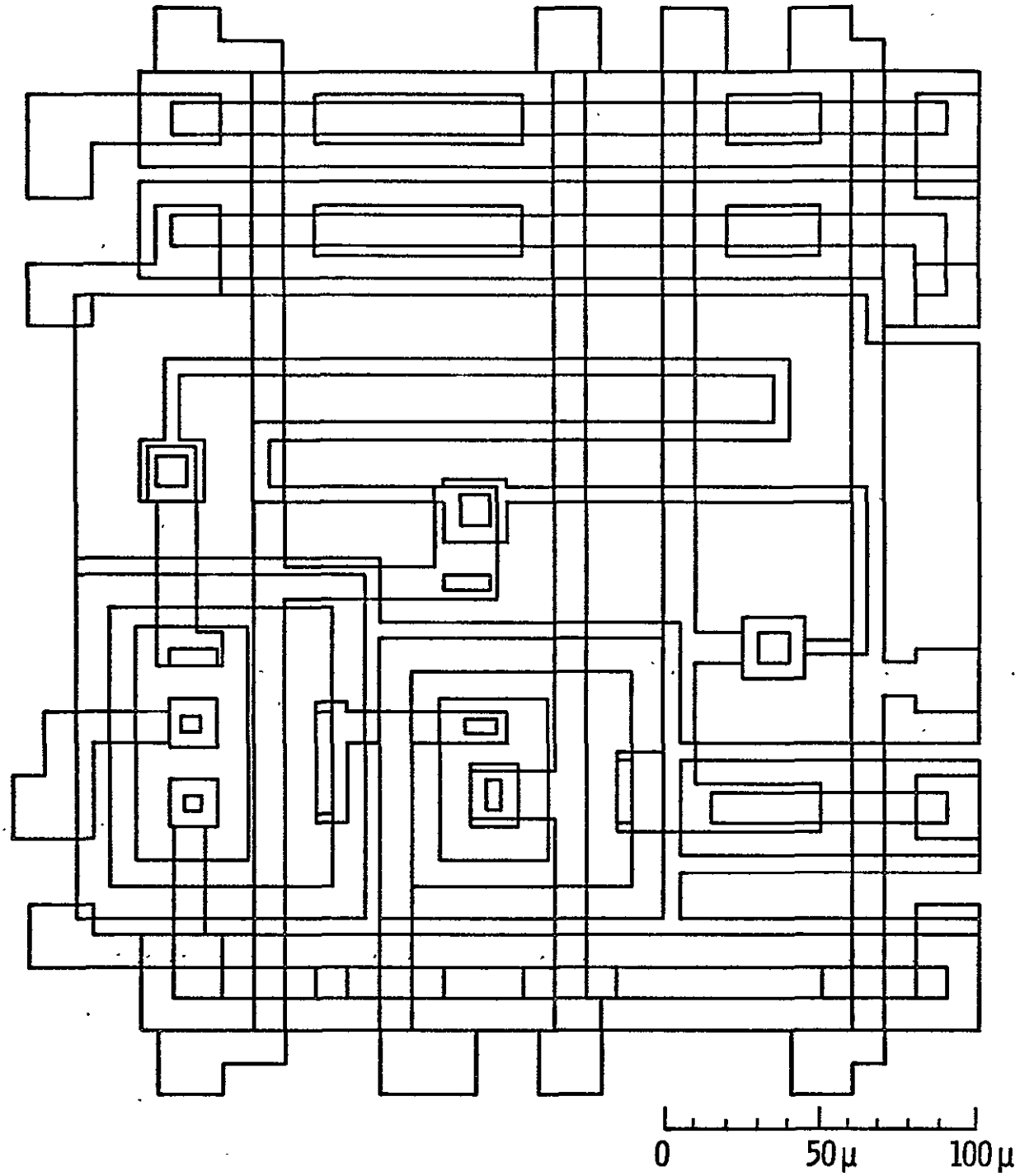


Fig. 2.4 T^2L NAND gate layout, first version

capacitance of each diffused undercrossing is $C_u \simeq 6.4 \times 10^{-17}$ Fd/μ^2 x 30 μ x 270 μ = 5.2×10^{13} Fd, and an average logic lead includes about 2 undercrossings. Therefore, the total capacitance associated with a typical logic lead is $(1.5 + 2 \times 5.2) \times 10^{-13}$ Fd = 1.2 pF. The time constant given by this in parallel with the 14 KΩ load resistor of the gate is 5 nS, giving a total gate speed for an average gate in the test vehicle of about 20 nS. The second version of this layout, shown in Fig. 2.5, was made to permit use of the bottom underdiffused lead independently of the lower gate input. This layout measured 234 μ x 312 μ, including probe test pads. It was designed for 240 μ x 320 μ spacings in a rectangular 4 x 6 array of similar cells. Some of the target specifications for the vertical profile and alignment tolerances for this gate are given in Table 4.

Substrate:	P-type, 10 Ω cm, 100 orientation, .010" thick
Subcollector:	N^+, As dopant, 4 μ drive, 20 $\Omega/\square$
Epitaxial Layer:	N-type, 4.5 μ thick, 5 Ω cm
Bases and Resistors:	P-type, 2.5 μ junction depth, 250 $\Omega/\square$
Emitters:	N^+, P dopant, 2.0 μ deep (0.5 μ base width)
Alignment Tolerances, Successive Patterns:	$\pm$ 2 microns

Gate Fabrication Specifications, Second Version

Table 2.4

A final modification of this layout was made in order to relax alignment tolerances, which were felt to be too stringent in view of the relatively large device geometry. This layout, which is shown in Fig. 2.6, measures 346 μ x 332 μ overall, and the test pads which

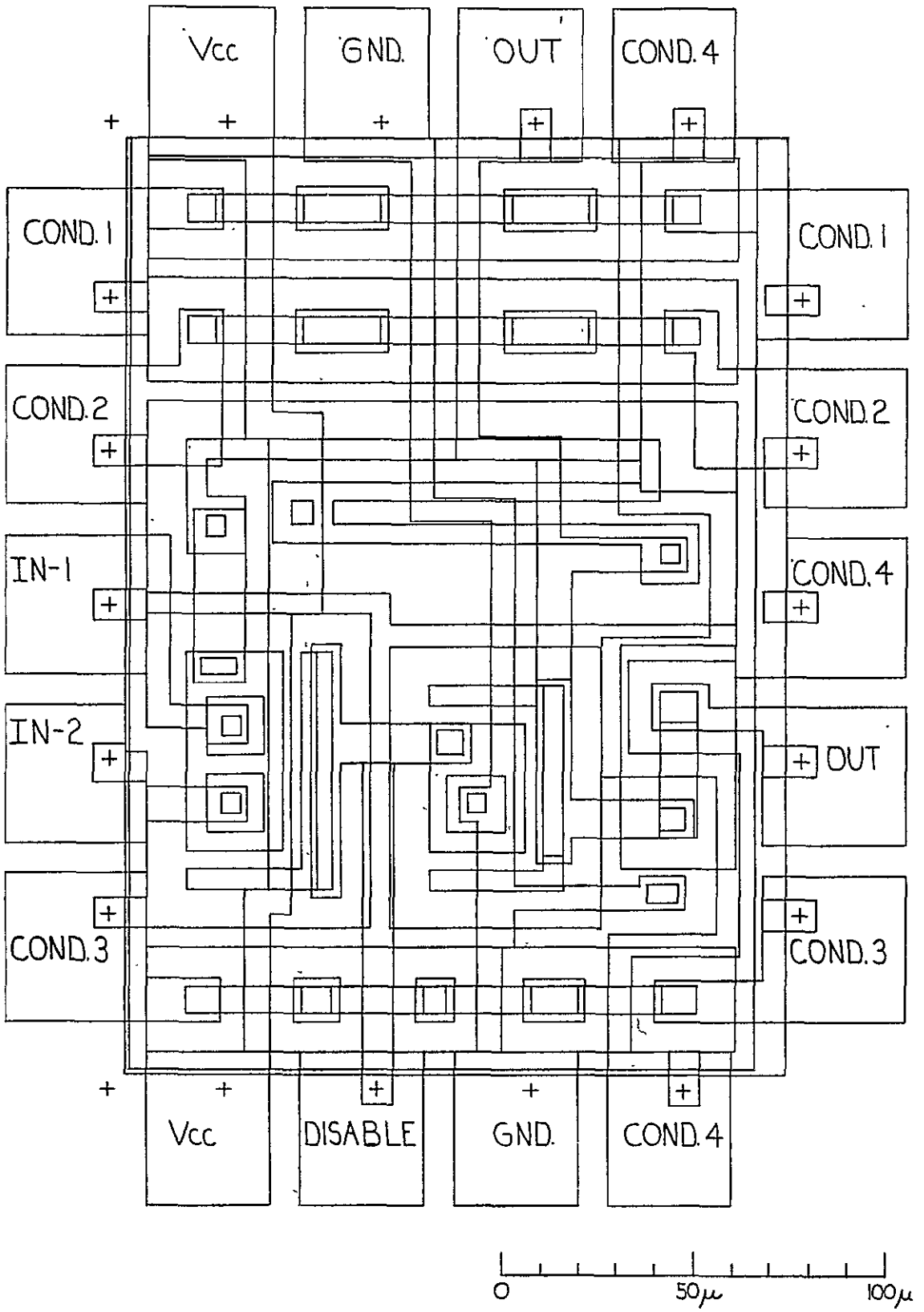


Fig. 2.5 T^2L NAND gate layout, second version

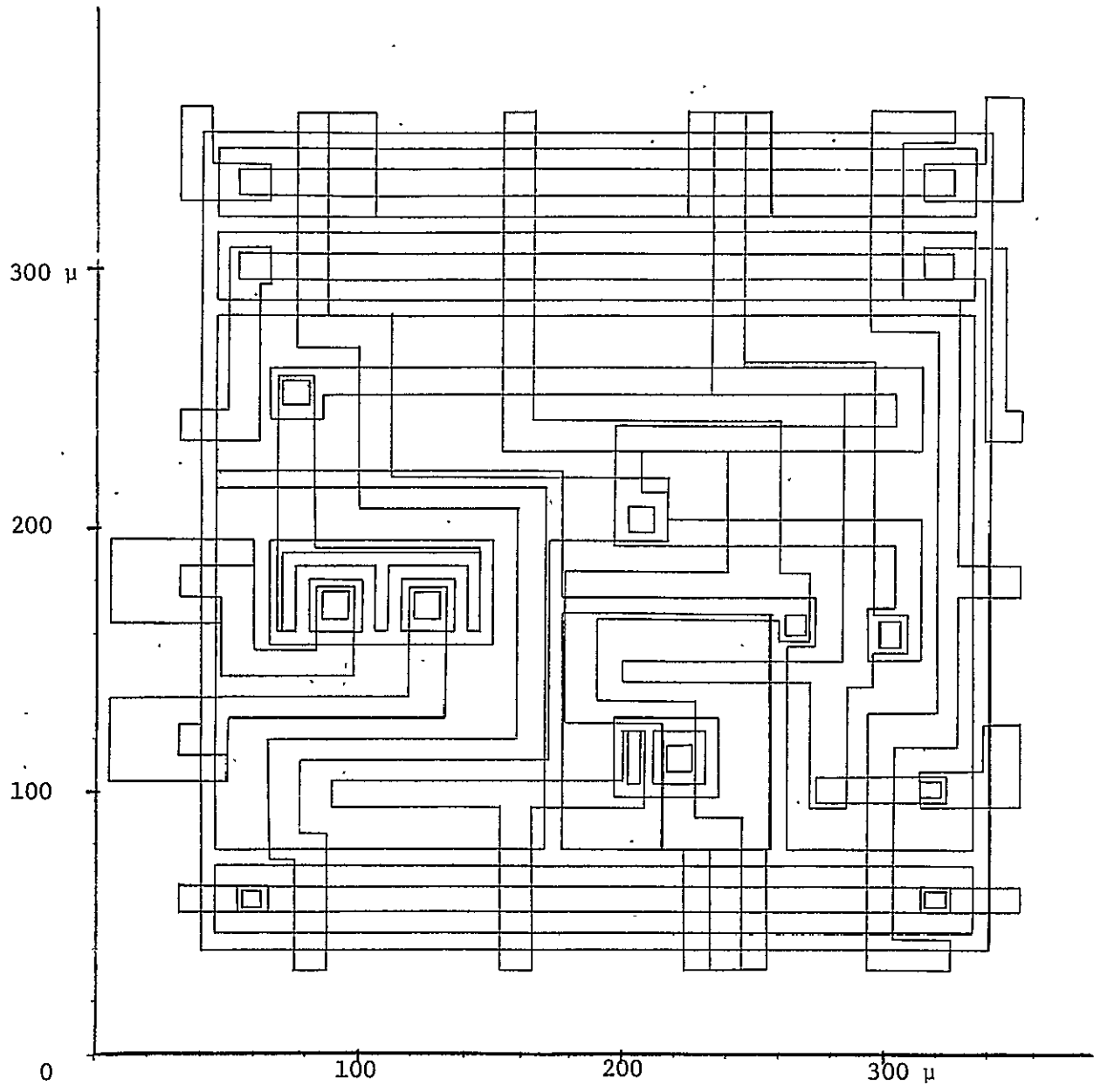


Fig. 2.6 T^2L NAND gate layout, final version

partly overly the circuitry clear the areas reserved for final interconnection. The larger size required a reduction of the array size to 4 x 4 to fit into the 2046 μ x 2048 μ raster available in the electron beam pattern generator. The vertical profile specifications for the final version are the same as for the second version (Table 2.4), but the alignment tolerance was relaxed to ± 5 μ.

2.3 1-BIT ADDER LAYOUT

A 3 x 4 array of NAND gates of which 10 gates are connected to make the one-bit adder are shown in Fig. 2.7. The logic signal interconnection paths shown here serve as the model for the discretionary wiring designs for an arbitrary subset of 10 gates from a larger array. In making the patterns for these gate arrays by the computer controlled scanning electron microscope, the number of gates that can be included in one exposure are limited by the number of points available in the X and Y directions of the scan, which originally was only 1,024. It was hoped at first that an array of 16 or 24 gates might be made by electronically moving the array of 4 gates into 4 or 6 different locations with sufficient accuracy that they might then be fabricated by proceeding in this fashion. Fig. 2.8 shows a 4 x 6 array of gates which was intended to be used in this way. The gates considered here were of the earlier type designed for spacing on 410 micron horizontal centers and 400 micron vertical centers, and the overall device size, as shown in Fig. 2.8, was 1875 microns high x 2750 microns wide. The patterns shown in Fig. 2.9 are the first metallization pattern for the array of 4 NAND gates which has been relocated at six different locations by

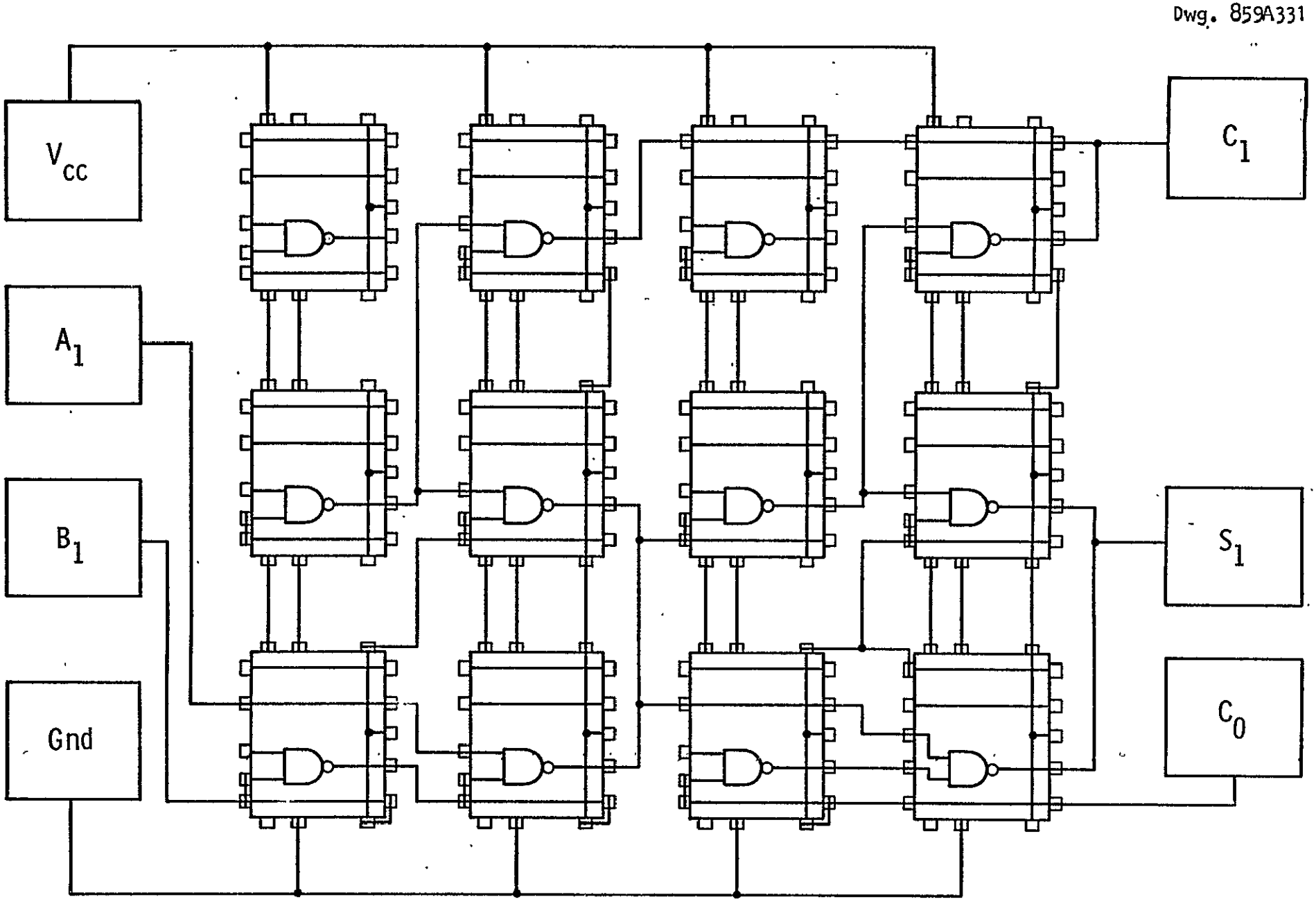


Figure 2.7 Model 10-gate layout for 1-bit adder

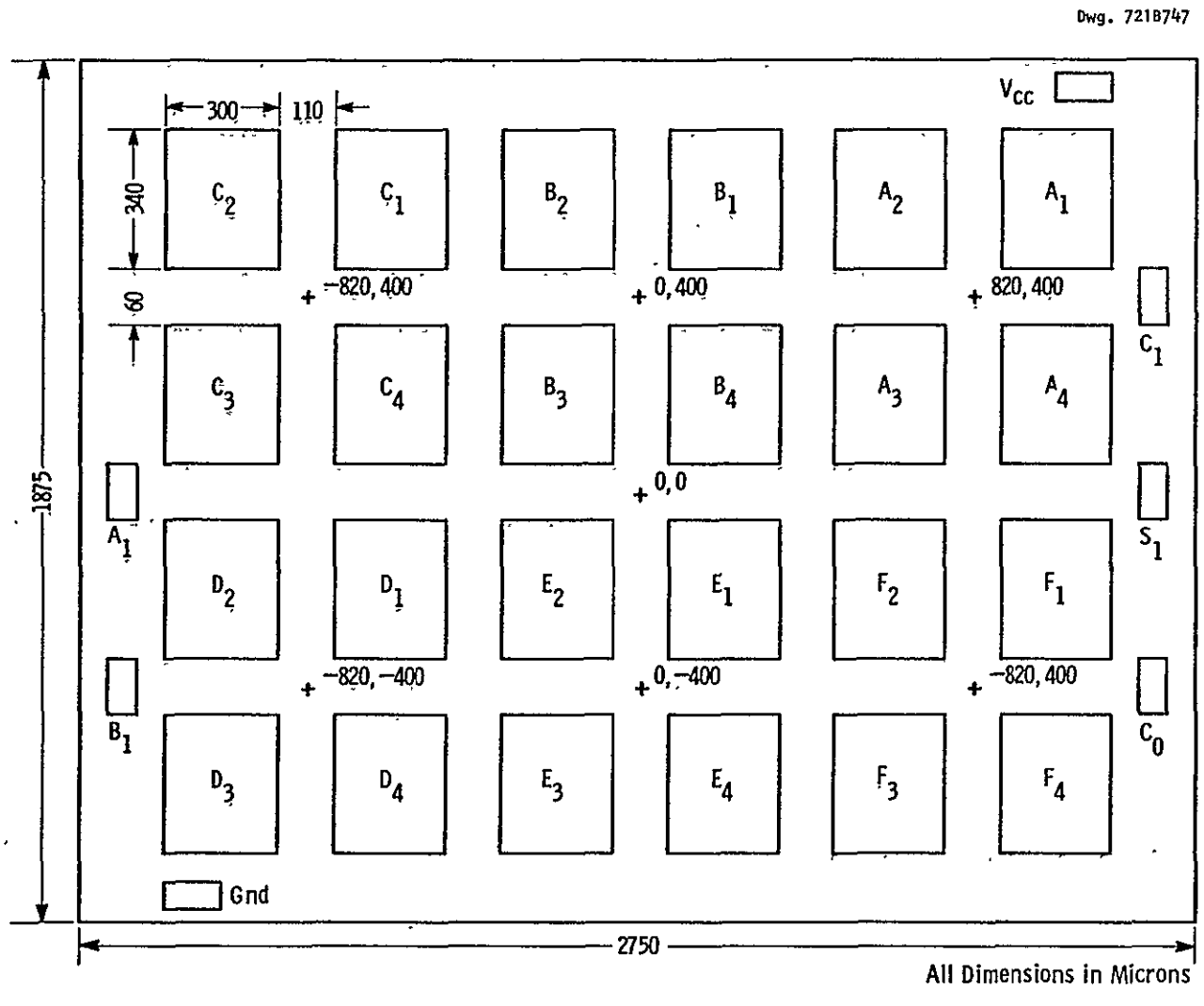


Fig. 2.8 Redundant layout of a 24-gate array for a 1-bit adder

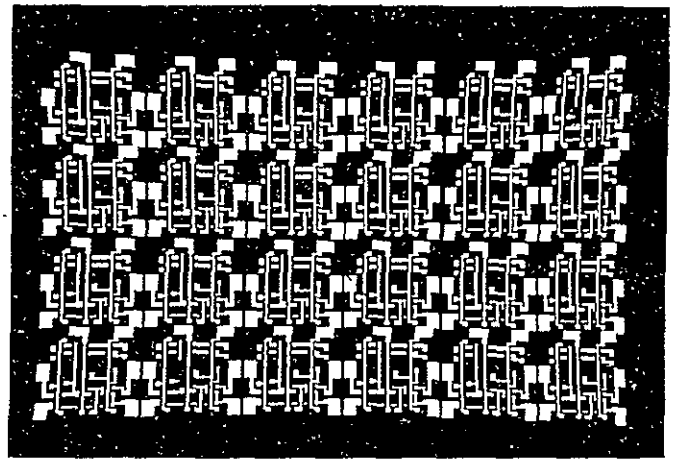


Fig. 2.9 24-gate first metal pattern

electronic repositioning. This was taken from a display on the face of a 5-inch cathode ray tube. Although the spacings seemed to be fairly well defined there was some undesired overlapping of metal at various places, and the matching of this to the final metal interconnect pattern, which was also designed for a raster using only a 1,024 address points in each axis, is shown in Fig. 2.10, wherein it will be noted that the logic interconnections frequently miss the intended connection pads at the device locations by an appreciable margin. This is primarily due to the fact that the two patterns, although produced by the same cathode ray tube, were produced on different scales. The contact pads shown were made using 1 micron as the basic point-to-point distance in the 1024 x 1024 raster, while the interconnections were made at a 4 times larger scale, that is, with the basic measure of length being 4 microns The distortion seen in Figure 2.10 originates in the cathode ray tube deflection system; distortion obtained in the scanning electron microscope is very much smaller than this, although of a similar type. In view of the difficulty in obtaining adequate registration between the overall final metal interconnection pattern produced at one scale and the device and initial metallization patterns produced at another scale, it was apparent that a larger address raster would be necessary, namely, a 4024 x 4024 point array, requiring a 12-bit X-address and a 12-bit Y-address. The final patterns included for production by the computer-controlled scanning electron microscope, now called the Electron Micropattern Generator, were made using such a 4096-square array of points. Use of these patterns with the 12-bit address system eliminated the

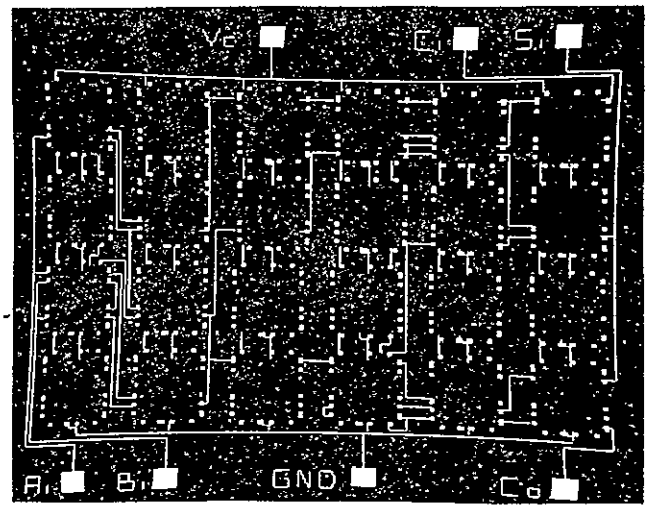


Fig. 2.10 10-gate adder interconnection (final metal)

loss of registration due to changes of scale, which are no longer required.

The 4 x 4 gate array of final design is laid out as indicated in Fig. 2.11. The initial carry input is made available at several points along the bottom edge of the device by means of diffused undercrossings to get across the ground bus. Also, the leads from the supply bus bonding pads are brought in to the gate array, and those from the signal bonding pads are terminated near the gate array so that the exposure for the discretionary, second metal pattern may be kept to a minimum. The overall device patterns are shown in Figs. 2.12 and 2.13 as written on a Tektronix 611 storage display unit by the digital interface of the Electron Micropattern Generator.

The complete device requires successive mask patterns to be exposed, developed, and processed, according to the following schedule:

Pattern No.	Description
1	Alignment marks for EMG and first optical alignment mark (large square)
2	Subcollector
3	P-Wall (Isolation Diffusion)
4	Base and Resistor Diffusion
5	Emitter, Contact Reinforcement, and Undercrossing N^+ Diffusion
6	Contact Openings
7	First Metal Interconnections
8	Final, Discretionary, Metal Interconnections

The last mask is not shown here, but is described and illustrated in the next section.

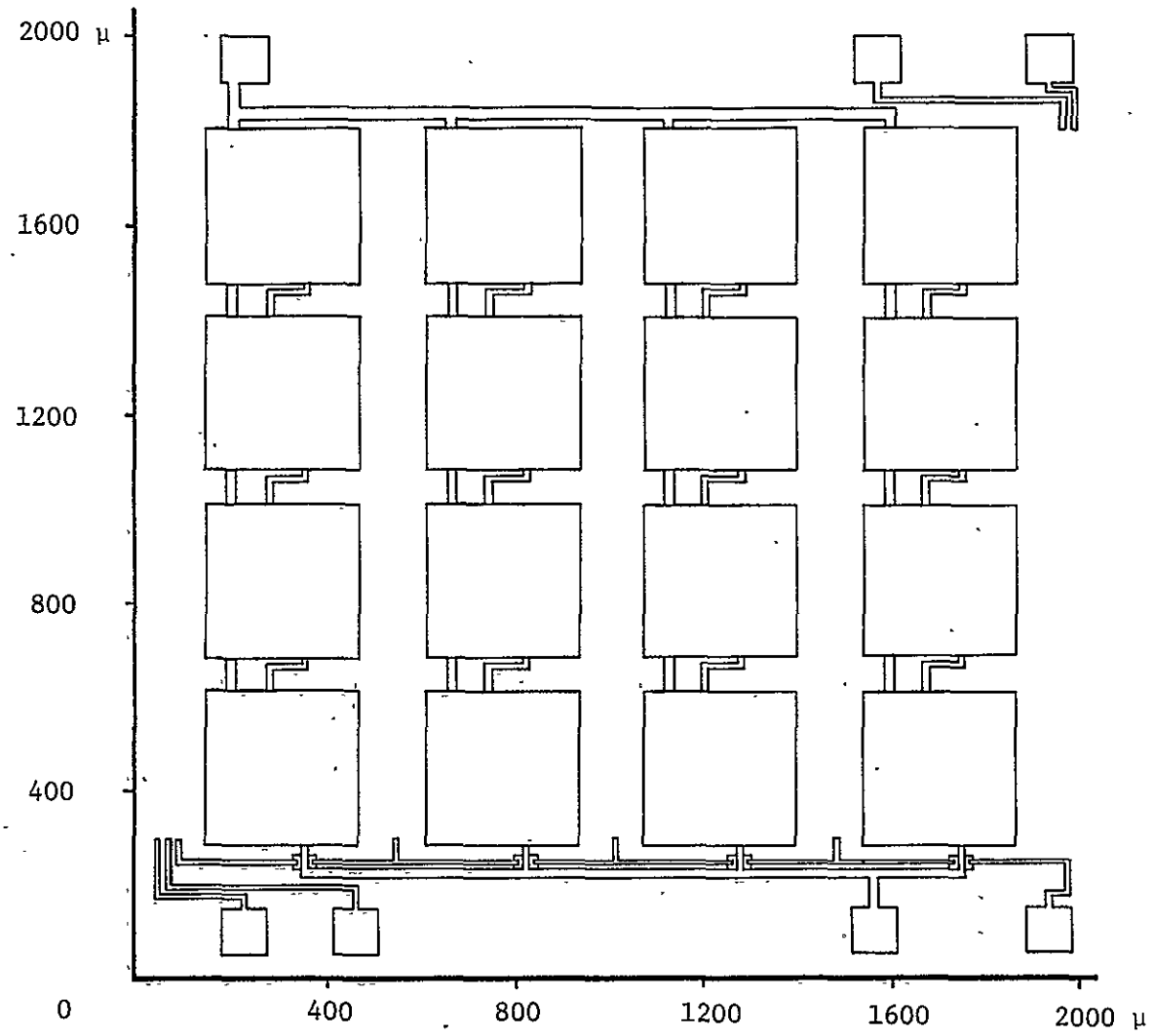
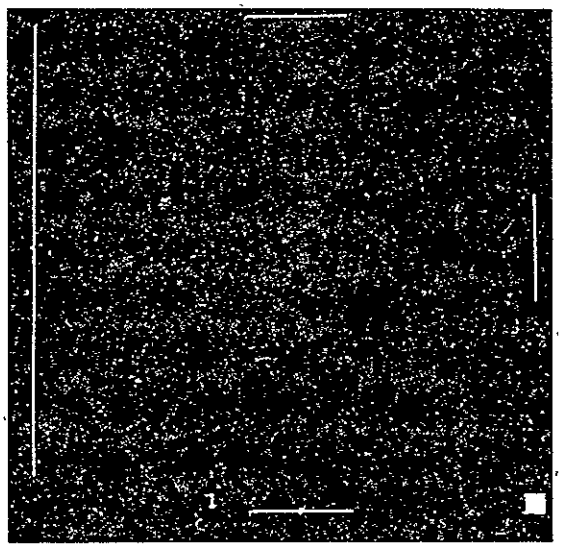
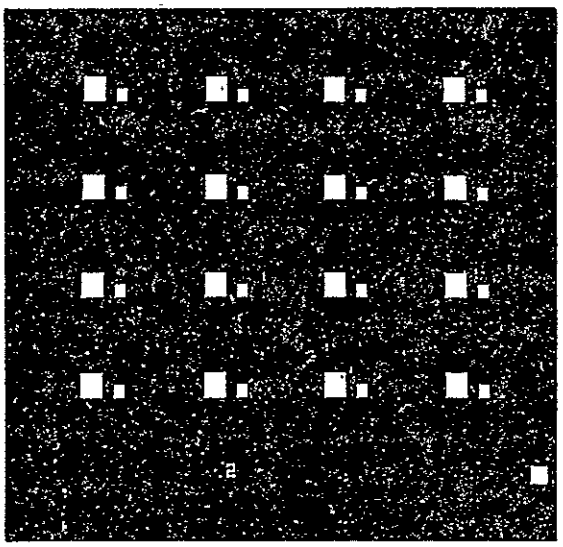


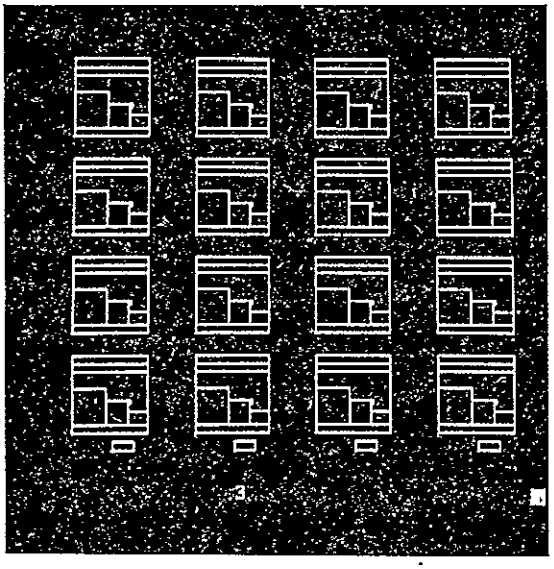
Fig. 2.11 16-gate array layout



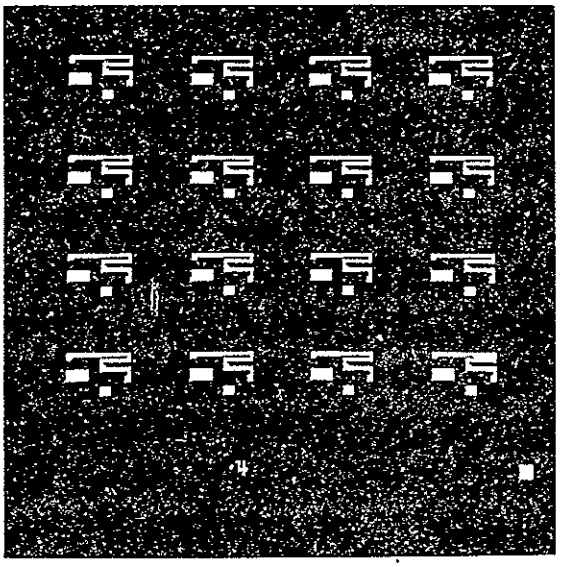
No. 1 - Alignment Marks



No. 2 - Subcollector



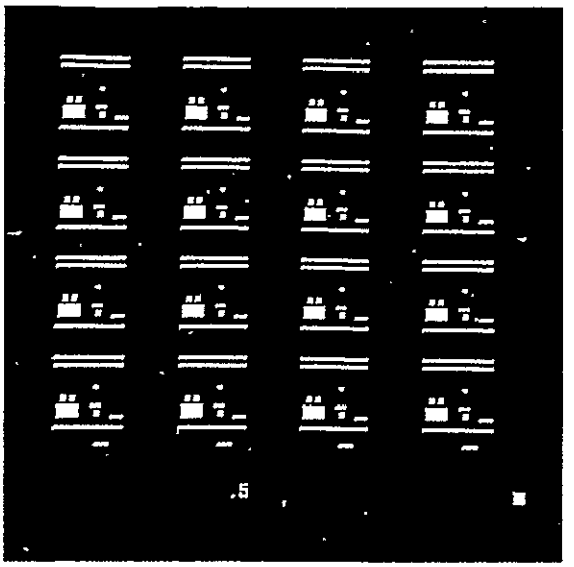
No. 3 - P-Well



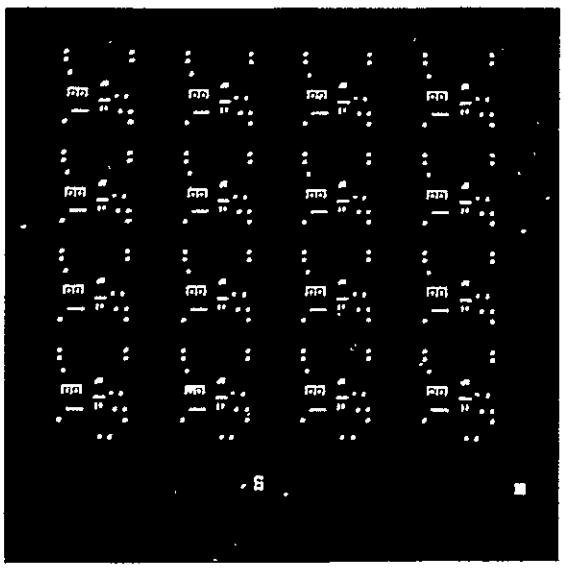
No. 4 - B and R

16-Gate Array Masks

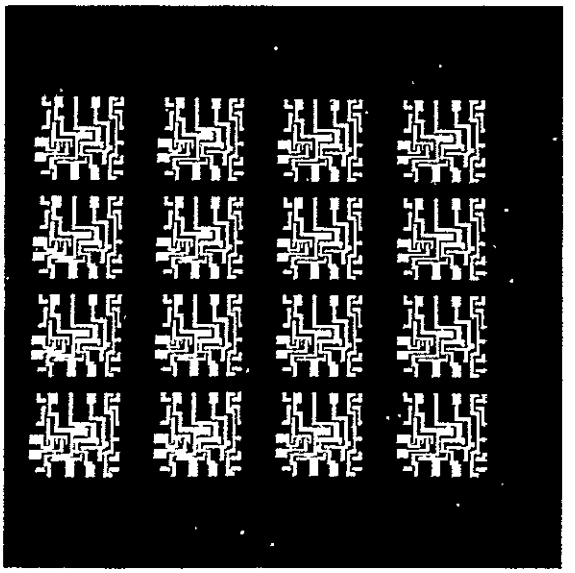
Fig. 2.12



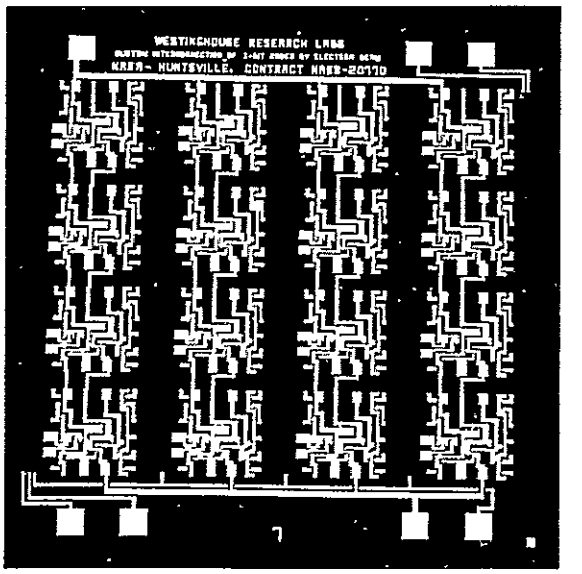
No. 5 – Emitter



No. 6 – Openings



No. 7 – First Metal, Gates Only

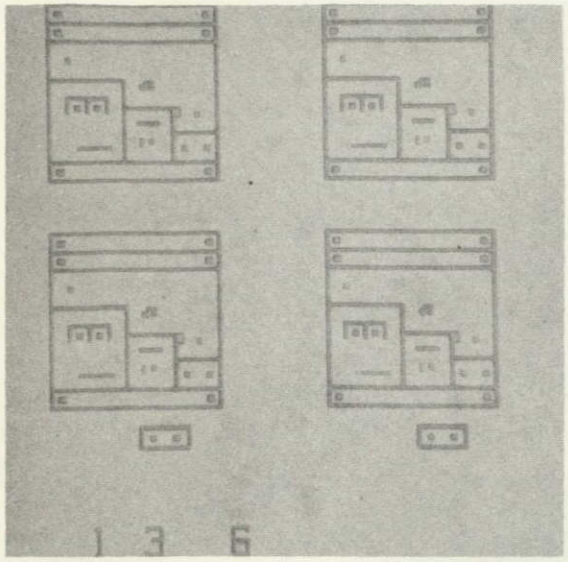


No. 7 – First Metal, With Pads and Title

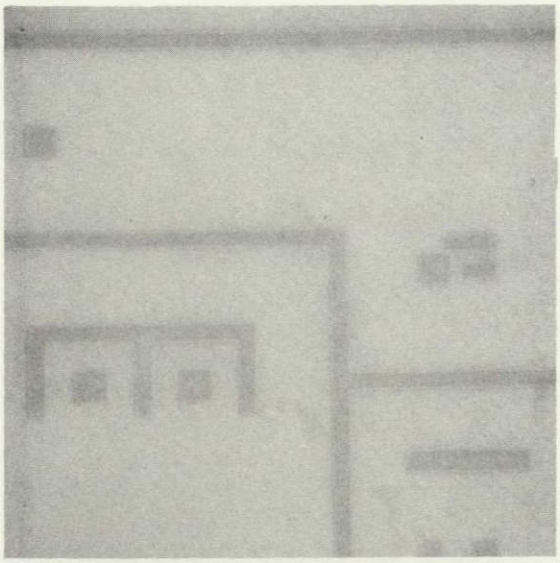
16-Gate Array Masks (Continued)

Fig. 2.13

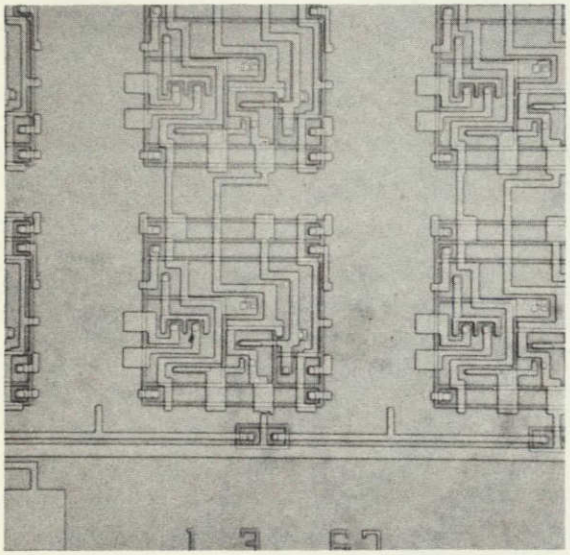
Fig. 2.14 and 2.15 show several microphotographs of the same patterns as holes etched in silicon dioxide, after exposure and development of the positive electroresist, plus overlaying subsequent patterns (No. 7 - 1st metal) in resist or aluminum which are in accurate registration with them.



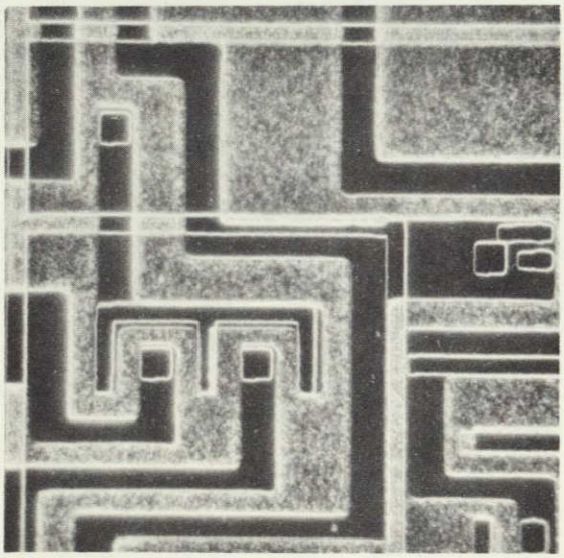
Nos. 1, 3 and 6 in SiO_2
Scale: 1 cm = 125 μ



Nos. 1, 3 and 6 in SiO_2
Scale: 1 cm = 20 μ



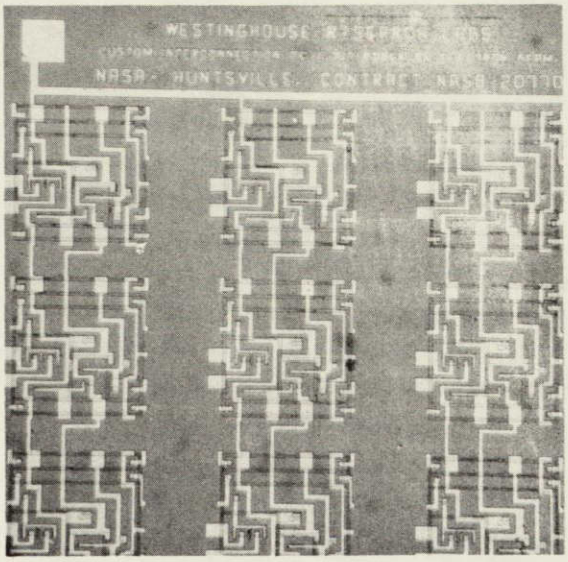
Nos. 1, 3 and 6 in SiO_2,
No. 7 in Electroresist
Scale: 1 cm = 125 μ



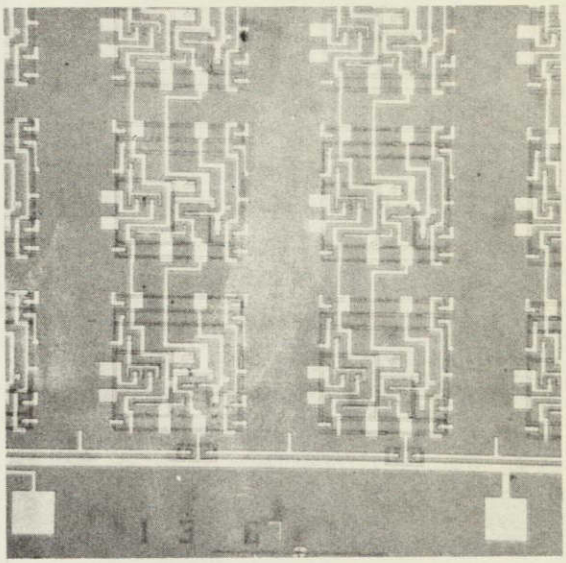
Nos. 1, 3 and 6 in SiO_2,
No. 7 in Electroresist,
Al Evaporated Overall
Scale: 1 cm = 20 μ

16-Gate Device Patterns in SiO_2 and Electroresist

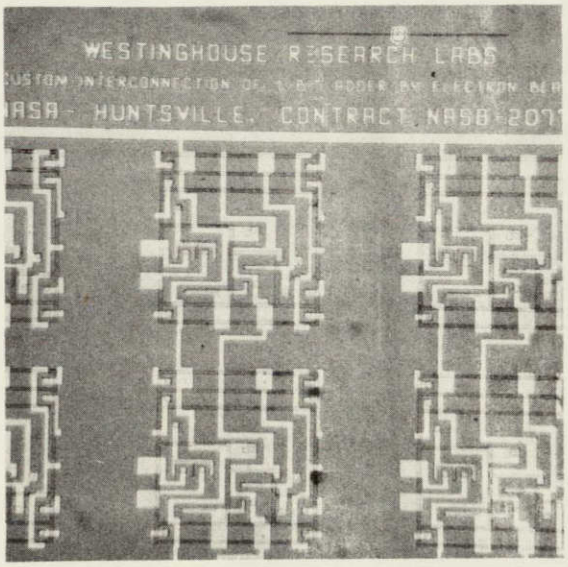
Fig. 2.14



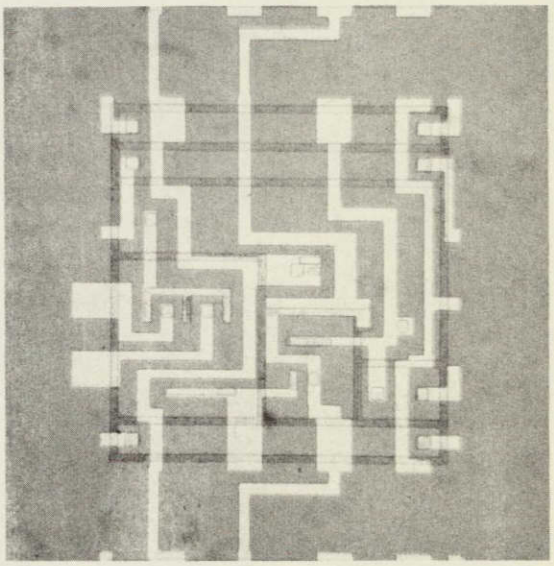
Nos. 1, 3 and 6 in Si02,
No. 7 in Al
Scale: 1 cm = 175 μ



Nos. 1, 3 and 6 in SiO_2,
No. 7 in Al
Scale: 1 cm = 175 μ



Nos. 1, 3 and 6 in SiO_2,
No. 7 in Al
Scale: 1 cm = 140 μ



Nos. 1, 3 and 6 in SiO_2,
No. 7 in Al
Scale: 1 cm = 70 μ

16-Gate Device Patterns in SiO_2 and Al

Fig. 2.15

3.0 DISCRETIONARY INTERCONNECTIONS

The present study has had as its goal the demonstration of a practical method of making, without the use of photomasks, final interconnections on an integrated circuit which are of custom design for that circuit only.

Two important uses of such custom metallization are: 1) fabrication of a variety of custom circuits starting with a standard array of circuit components, as in the "masterslice" approach, and 2) the accommodation of defects on a given integrated circuit by wafer testing (at the subcircuit level) followed by interconnection of good elements according to a computer-derived metallization geometry matched to the array of good elements.

The latter application is an important procedure in defect accommodation techniques required for the realization of large, high-reliability systems on a silicon monolithic substrate, and in view of NASA's interest in reliability aspects of advanced electronic systems, it was chosen for a demonstration of the custom interconnection method to be developed. Two simplifying ground rules were adopted in the present study: 1) testing of interconnected cells on the wafer was to be done by mechanical probes, as compared with electron beam probing methods required for maximum density circuits, and 2) only a single level of metal was to be used, as compared with the multilevel approach needed for systems applications. Pre-placed diffused undercrossings were adopted as the means for accomplishing lead crossings in the final interconnection paths.

The work performed in this area can be divided roughly into two parts: 1) developing techniques for putting second, final metallization over and in contact with the first, intracell, metallization in the desired pattern, and 2) developing suitable computer programs for laying out the required interconnections of good cells. These parts are discussed in the following two sections.

3.1 METALLIZATION METHOD

Two basic approaches to providing the final metallization steps were investigated, namely the use of a positive resist as a rejection mask, and the use of a negative resist in the conventional manner as an etch resist. Both methods preserve the initial, intracell metallization intact, except for the probe test pads, through use of an intermediate protective resist step. A third method which involved stripping the initial metallization completely and then reproducing it plus the custom interconnections, was discarded because of the lack of confidence which could be placed on the new and untested intracell connections.

The positive resist method considered involved 6 steps (see Fig. 3.1). After probe test of the unit cells, intraconnected and provided with probe test pads, a negative resist is applied, exposed over the unit cell areas and developed and etched, thereby removing the test pads (steps 1 and 2). (Alternatively, a positive resist, exposed in the areas of the test pads and developed, could be used.) This resist is then removed and a positive resist applied. The latter is exposed along the custom interconnection routes and developed, thereby creating a rejection mask (step 4). An aluminum layer is then deposited (step 5), making contact to the first metallization or attaching to the

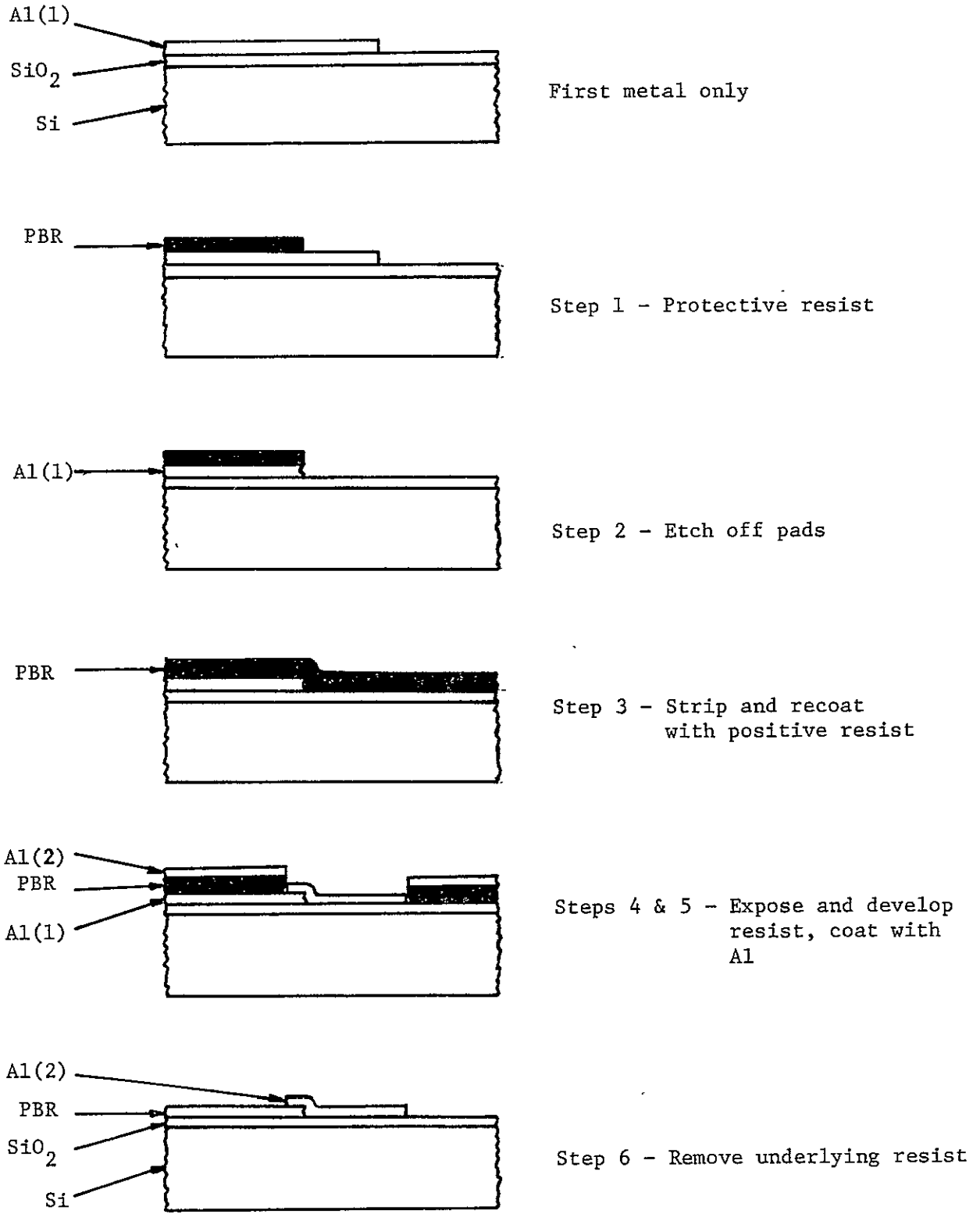


Fig. 3.1 Positive resist, rejection mask, 2nd metal method

oxide, only at the exposed and developed areas. Subsequent stripping of the remaining, underlying resist or rejection mask (step 6) then serves to remove the undesired metal, leaving the desired final metallization pattern. Steps 3 through 6 of this process were carried out on aluminum conductors on SiO_2; the resulting conductive paths showed good adhesion, fair edge definition, but poor electrical contact to underlying metal. The second metal showed breaks along the edges of the first metal pattern, and the conduction path was interrupted at those areas (see Fig. 3.4-a).

The negative resist method consists of six principal steps also (see Fig. 3.2). After the probe test, a negative resist is deposited, exposed over the unit cell areas, and developed, thereby providing a protective coat over the intraconnected, tested cells, but exposing the test pads (step 1). The final aluminum layer is next deposited, and then negative resist (steps 2 and 3). The resist is exposed along the desired interconnection routes, including a small overlap into the protected areas, and at the wire bond areas (step 4). Subsequent development, etching of the aluminum, and removal of the resist results in the desired circuit (steps 5 and 6). This procedure was also tried, and yielded very good results. The final metal pattern had good edge resolution, good adhesion, showed no breaks over oxide or metal steps, and showed good conduction to the first metal pattern (see Fig. 3.4-b). It has, however, the distinct disadvantage of leaving a bit of aluminum projecting upward where the final metal overlayed the original metal, which might give low resistance to abrasion.

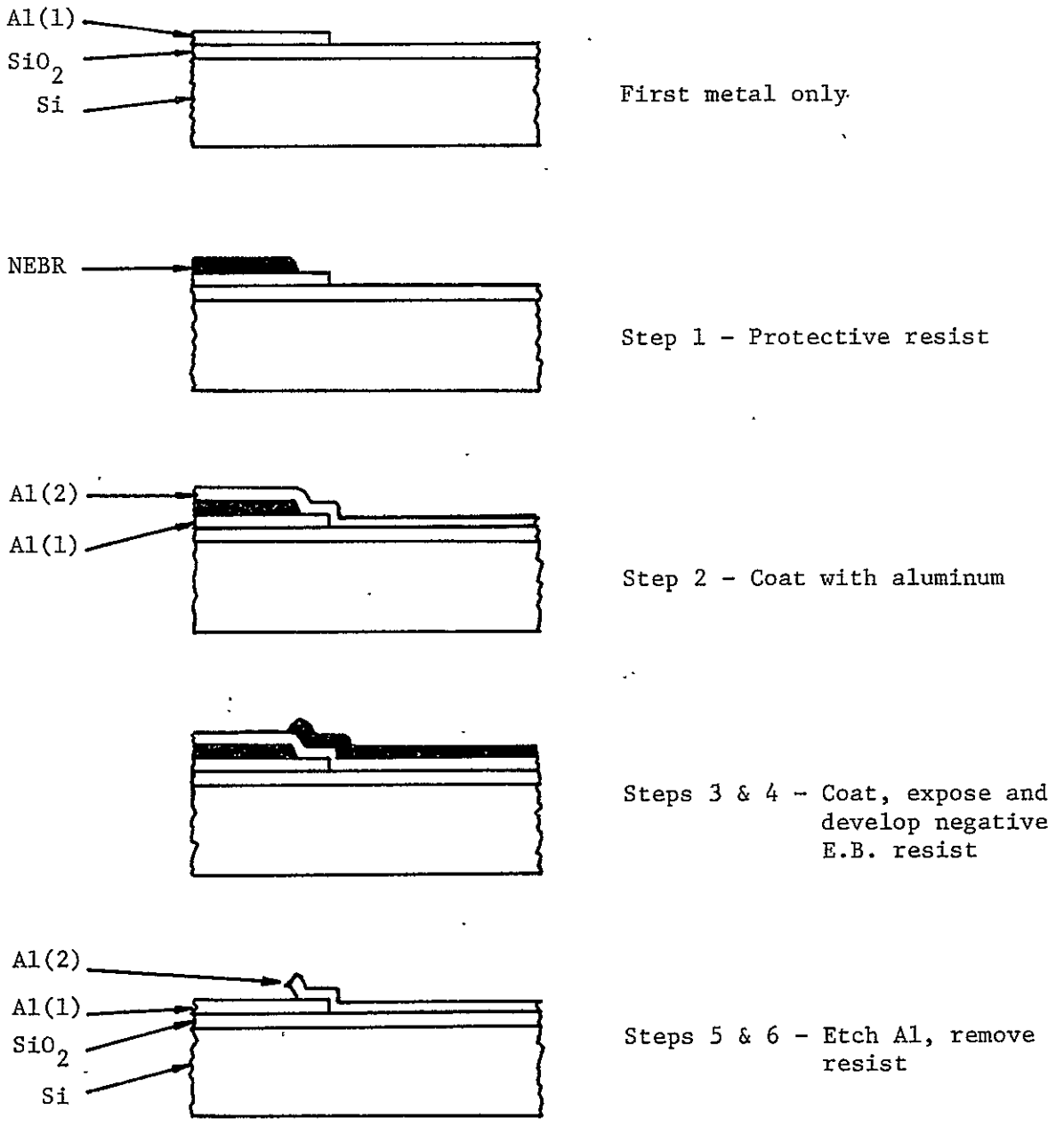


Fig. 3.2 Negative resist, second metal method

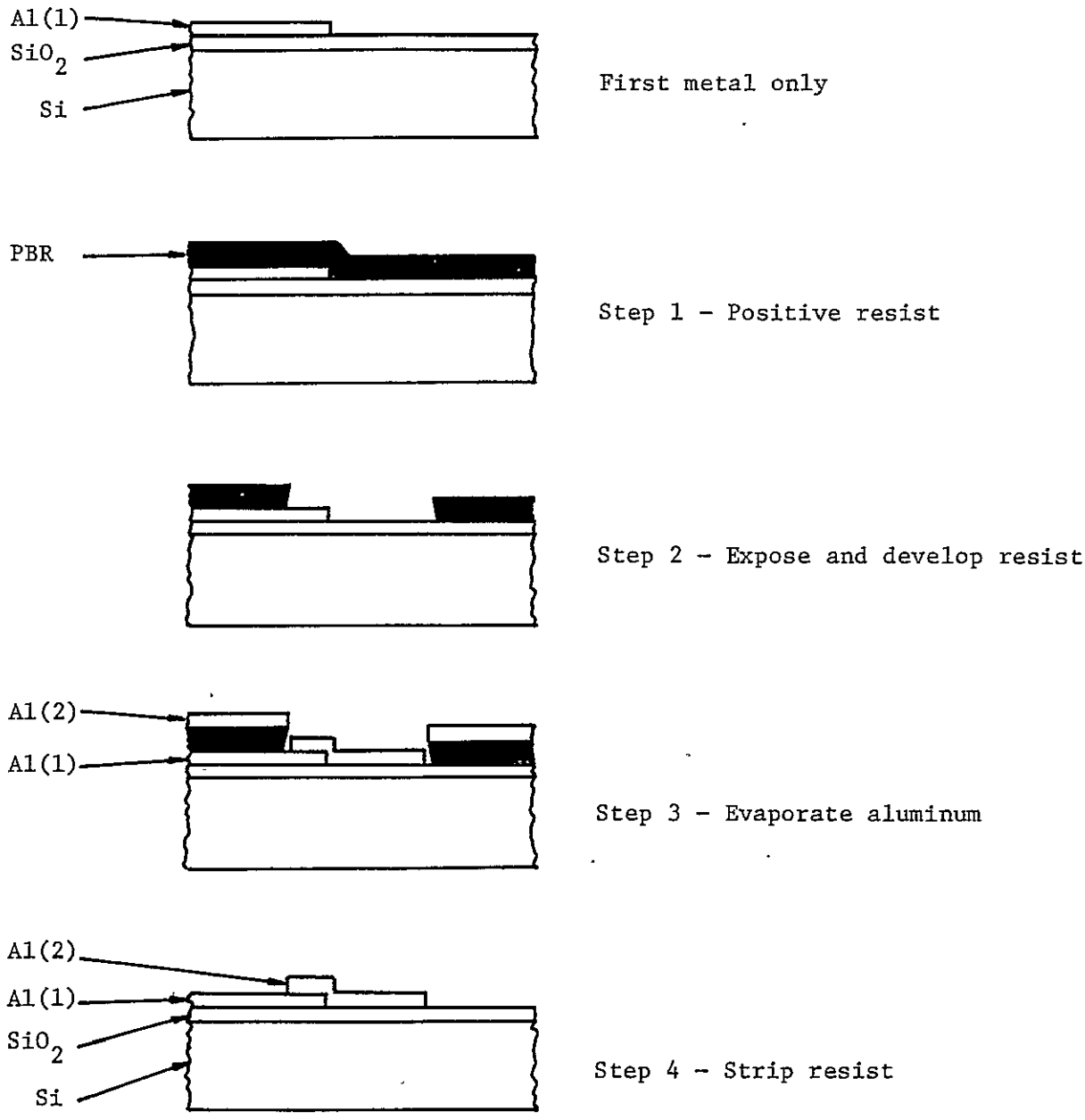
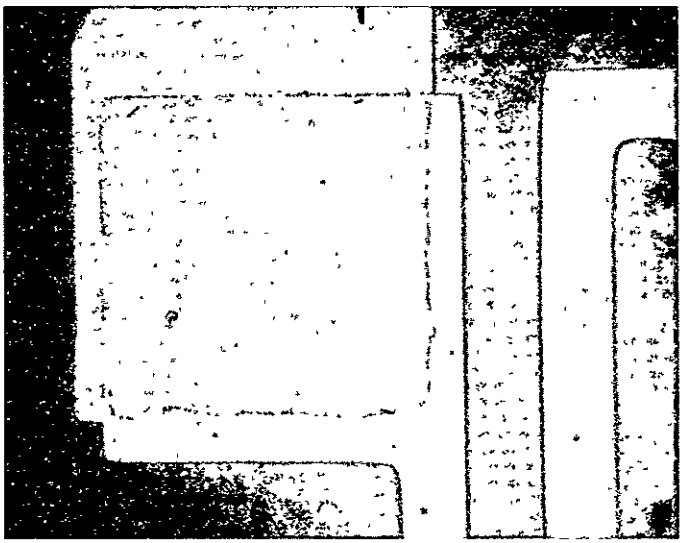
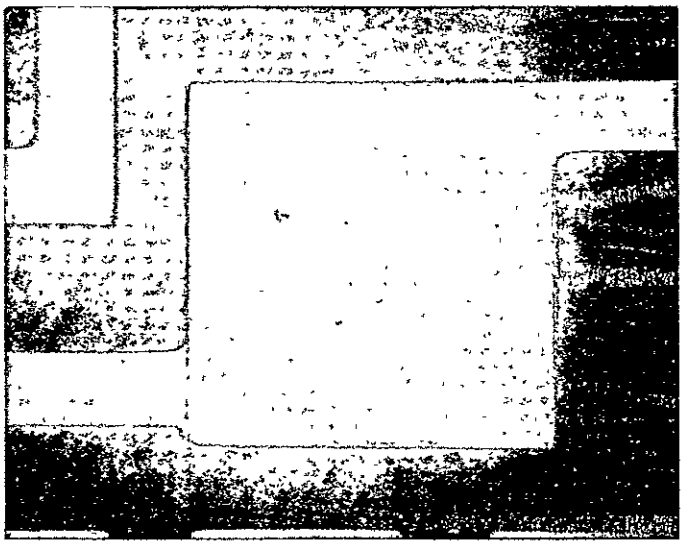


Fig. 3.3 Positive resist, rejection method, without protective resist



a) Using Positive Resist for Rejection



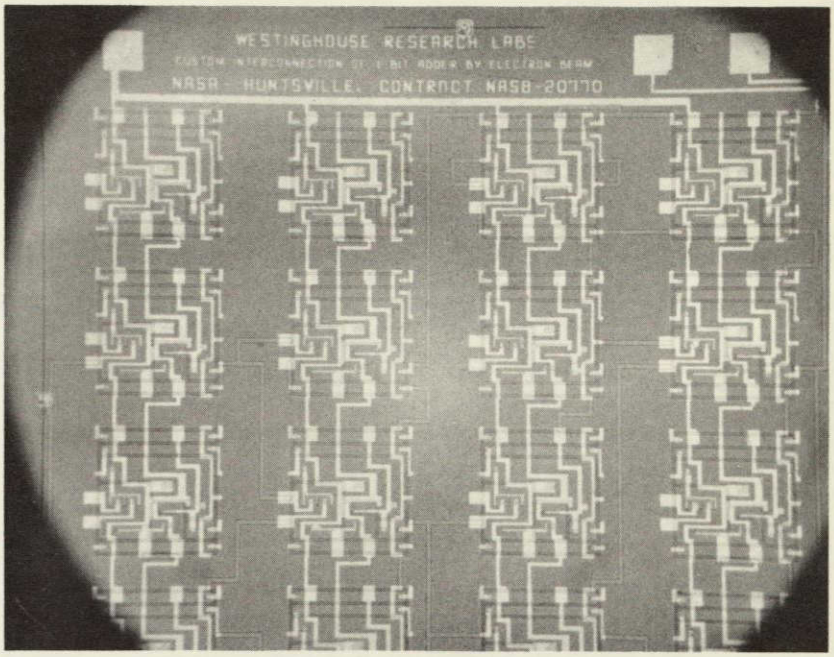
b) Using Negative Resist for Etching

Fig. 3.4 Metallization Technique

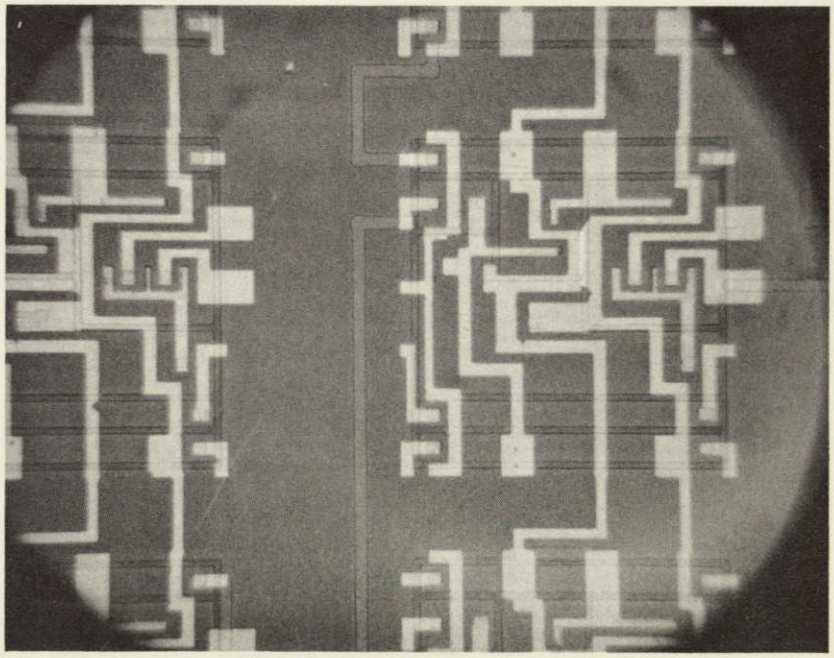
A variation of the positive resist method was permitted by the patterns finally used which did not require removal of the large test pad areas since they did not project into the final metal areas, but were designed into the gate area. This method, shown in Fig. 3.3, does not require a protective resist step, and only involved coating with positive electroresist, exposing the interconnection pattern, developing, evaporating the aluminum conductor, and stripping the resist. Because of the slight overhang provided by positive electroresist after development, high quality line resolution and edge smoothness is provided by this method, as long as the resist thickness is appreciably greater than the metal thickness. When this is the case, a clean break in the conductor edge is possible during the removal of the resist and unwanted metal.

Other benefits of this technique include the latitude of time permitted for the rejection process since no desired material is being attached, the absence of undercutting effects, and the flatness of the final conductors, with no protruding edges. In this process, good continuity of connections over the edges of the initial conductors, where the final metal laps them, requires that the final metal be appreciably thicker than the initial metal.

It should be noted that adhesion is a principle problem in this method, and it has not been resolved satisfactorily in the present program. Fig. 3.5 shows the first metal pattern in aluminum aligned with earlier patterns in SiO_2, and with the final metal pattern exposed in registration with those and developed. The discretionary



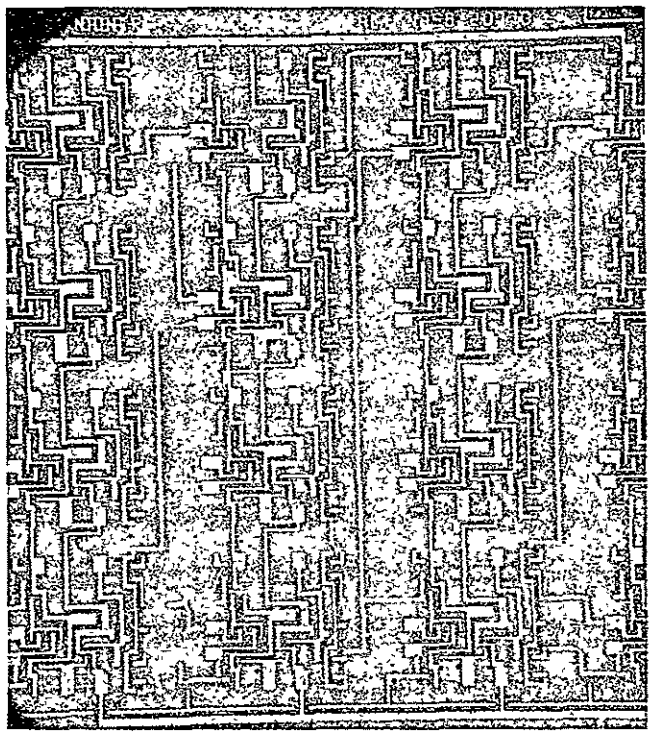
a) First Metal Pattern in Al, Final Metal Pattern in Positive Electroresist
(Scale: 1 cm = 200 μ)



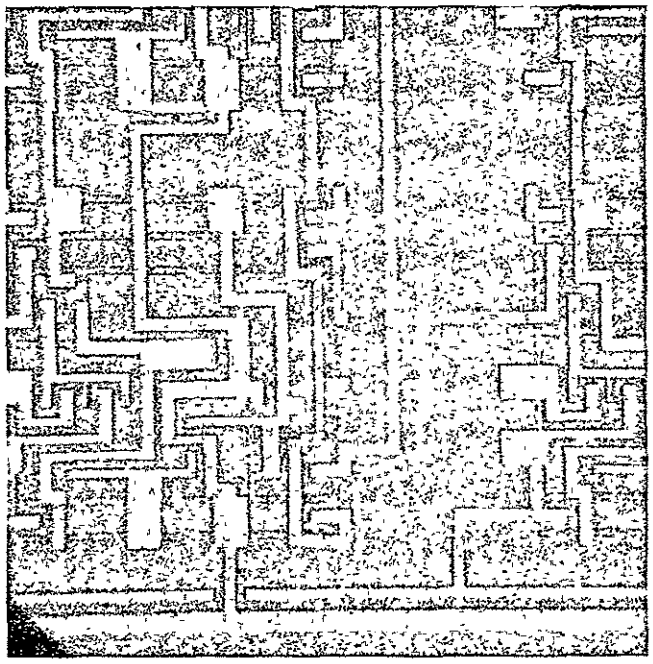
b) First Metal Pattern in Al, Final Metal Pattern in Positive Electroresist
(Scale: 1 cm = 70 μ

Fig. 3.5 Metallization Technique, EMG-Exposed Patterns

interconnection pattern of this figure corresponds with the solution of test case 401 illustrated in Fig. 3.19 of the following section. An example of the final metallization provided by this is shown in Fig. 3.6 (corresponding to test case 201, Fig. 3.17), wherein it may be seen that not all of the desired leads remained in place through the rejection process. Solution of this problem will require an improved surface preparation immediately prior to the metal deposition, possibly through the use of R.F. sputter etching.



a) Scale: 1 cm = 200 μ



b) Scale: 1 cm = 70 μ

Fig. 3.6 Metallization Technique - Microphotographs of First and Second Metal

3.2. SOFTWARE

Two computer programs were developed to provide the custom interconnection patterns required in this program to connect viable gates into the configuration of a 1-bit adder. The first has broad generality, and selects an optimum and connectible set of the required number of units from a given set of operable units. The name of this program is SELECT/SET. The second program determines lead routings for the selected set of units according to the model diagram. The basic algorithm for this second program, which is called CIRCUIT/SIGNALS, also has general application, but requires a bit of adaptation to the crossover possibilities provided for in the redundant array. The output of the second program is translated into the proper format and scale for the SEMTAPE/COMPILE software which generates the digital control tape for the Electron Micropattern Generator. The two programs, SELECT/SET and CIRCUIT/SIGNALS, are described below.

3.2.1. SELECT/SET

A program, SELECT/SET, has been written to select a wireable set of elements out of the given good elements on a chip. It is the first one of the series of programs developed to write magnetic tapes for discretionary interconnections. The Electron Micropattern Generator (EMG) uses these tapes to draw integrated circuits. The elements on the chip are arranged in the form of an m x n array. The circuit is described with respect to an ideal p x q array of good elements. m x n is taken adequately larger than p x q to assure availability of the required number of good elements. The program selects a set of good elements on the chip, topologically similar to the ideal array.

ALGORITHM

The process of selecting a useable set of good elements consist of four steps. The first step examines the chip for the number of good elements required by the circuit. The second step finds C_s, a p x q subarray of C with the maximum number of good elements. Step three assigns one good element from outside C_s to each bad element in C_s to complete a set of p x q good elements. The last step orders the elements of the set to produce a topological isomorphism between the set of good elements and the ideal array.

In the first step each element is examined and the number of good elements is counted. Chips having less than p x q good elements are rejected.

In the second step, a p x q subarray C_s is obtained from C by deleting certain rows and certain columns in s = (m-p) + (n-q) stages (see Figs. 3.7 and 3.8).

At stage λ an m_λ x n_λ array C_λ is obtained from $C_{\lambda-1}$ (λ = 1, 2, x ... S. C_o = C) as follows:

Let G_{Ri} be the number of good elements in the i^{th} row and G_{Cj} be the number of good elements in j^{th} column of $C_{\lambda-1}$. And let

$$G_{RK} = \text{Min } \{ G_{Ri},\ i=1,2,....m_{\lambda-1}\}$$

and

$$G_{CL} = \text{Min } \{ G_{Cj},\ j = 1,\ 2,\ \ldots\ n_{\lambda-1}\}$$

Now if $m_{\lambda-1} > p$ and $\frac{G_{RK}}{n} < \frac{G_{CL}}{m}$ or $n_{\lambda-1} = q$

Let $m = 6$ $n = 5$ and $p = q = 4$

and let $C =$

1 1 0 1 1
0 1 1 1 0
1 0 1 0 1
1 0 0 1 0
0 1 1 0 0
1 0 0 0 1

Number of good elements = 16 ($\geq 4 \times 4 = 16$)

End of Step 1

STEP 2

$S = (6 - 4) + (5 - 4) = 3$

and $C = C_o =$

1 1 0 1 1
0 1 1 1 0
1 0 1 0 1
1 0 0 1 0
0 1 1 0 0
1 0 0 0 1

$\therefore$ $G_{RK} = 2$ and $G_{CL} = 3$

$\rightarrow$ $C_1 =$

1 1 0 1 1
0 1 1 1 0
1 0 1 0 1
1 0 0 1 0
0 1 1 0 0
1 0 0 0 1

SELECT/SET - Steps 1 and 2

Fig. 3.7

here $G_{RK} = 2$ and $G_{CL} = 2$

$\rightarrow$ $C_2 =$

1	1	0	1	1
0	1	1	1	0
1	0	1	0	1
1	0	0	1	0
0	1	1	0	0
1	0	0	0	1

here $G_{RK} = 2$ and $G_{CL} = 3$

$\rightarrow$ $C_s = C_3 =$

1	1	0	1	1
0	1	1	1	0
1	0	1	0	1
1	0	0	1	0
0	1	1	0	0
1	0	0	0	1

End of Step 2

SELECT/SET - Completion of Step 2

Fig. 3.8

then delete the K^{th} row else delete the L^{th} column from the array $C_{\lambda-1}$. Define C_λ as the remaining part of $C_{\lambda-1}$ and reindex the rows and columns of C_λ.

In C_s, the selected p x q portion of C, the rows and columns may not be consecutive. No complete row of C is in C_s unless q=n and no complete column of C is in C_s unless p=m.

The third step in the alorithm consists of assigning one good element from outside C_s to each bad element in C_s, if any. The indices of good elements in C_s and those of the assigned elements are stored in a p x q array C^* at respective places (see Figs. 3.9 and 3.10). The assignment is done iteratively, as follows:

At a given stage, let B_{Ri} be the number of bad elements in the i^{th} row and let B_{Cj} be the number of bad elements in the j^{th} column of C within the selected set, C_s.

Let

$$B_{RK} = \text{Min } \{B_{Ri} | B_{Ri} \neq 0,\ i=1,2,\ldots m\}$$

and

$$B_{CL} = \text{Min } \{B_{Cj} | B_{Cj} \neq 0,\ j=1,2,\ldots .n\}.$$

If $B_{RK} < B_{CL}$ then pick the leftmost bad element in the K^{th} row else pick the uppermost bad element in the L^{th} column of C in C_s. Let the element be c_{ij}. If available, a good element from outside of C_s but in the i^{th} row or the j^{th} column is assigned to c_{ij}. Any such good element is assigned to only one bad element. If no such good element is available, an imaginary element I_{ij} is assigned to c_{ij}. This process is repeated until an assignment has been made to every bad element in C_s.

C_s =

1	1	0	1	1
0	1	1	1	0
1	0	1	0	1
1	0	0	1	0
0	1	1	0	0
1	0	0	0	1

and C^* = 1,1 1,2 1,4
2,2 2,3 2,4
3,1 3,3
4,1 4,4

C_s =

1	1	0	1	1
0	1	1	1	0
1	0	1	0	1
1	0	0	1	0
0	1	1	0	0
1	0	0	0	1

and C^* = 1,1 1,2 1,5 1,4
2,2 2,3 2,4
3,1 3,3
4,1 4,4

C_s =

1	1	0	1	1
0	1	1	1	0
1	0	1	0	1
1	0	0	1	0
0	1	1	0	0
1	0	0	0	1

and C^* = 1,1 1,2 1,5 1,4
6,1 2,2 2,3 2,4
3,1 3,3
4,1 4,4

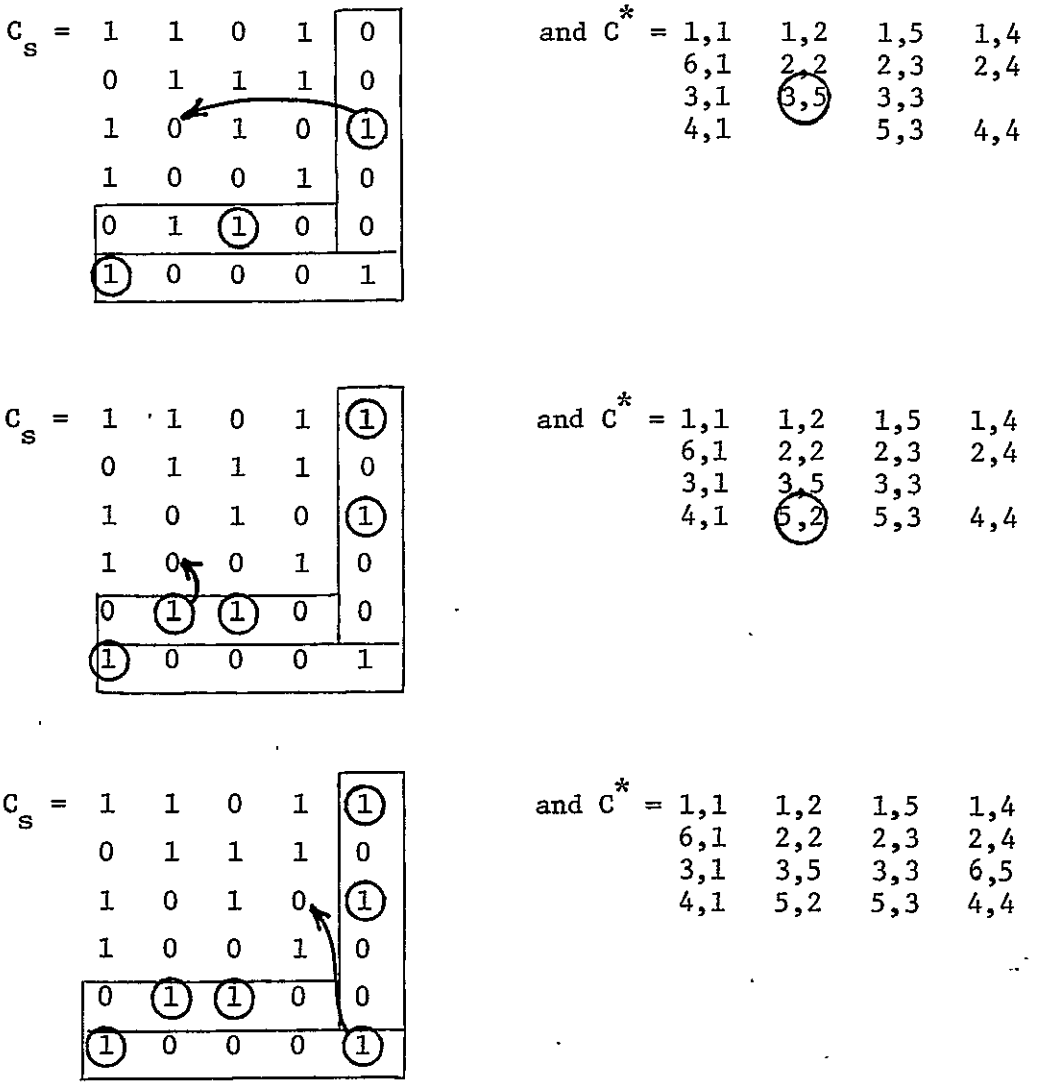
C_s =

1	1	0	1	1
0	1	1	1	0
1	0	1	0	1
1	0	0	1	0
0	1	1	0	0
1	0	0	0	1

and C^* = 1,1 1,2 1,5 1,4
6,1 2,2 2,3 2,4
3,1 3,3
4,1 5,3 4,4

SELECT/SET - Step 3

Fig. 3.9



SELECT/SET - Completion of Step 3

End of Step 3.

Fig. 3.10

To complete the third step the following part of the algorithm consists of replacing each imaginary element, if there are any at the end of the above process, with a good element.

Let the imaginary element be I_{ij}. We first search for an unassigned good element in the part of the $(i-1)^{th}$ row of C which is not in subarray C_s. If no such element is available in the $(i-1)^{th}$ row a similar search is made in the $(i+1)^{th}$ row. If one is not found we search for such an element in the $(j-1)^{th}$ and the $(j+1)^{th}$ column of C, respectively. The search is continued through the $(i-k)^{th}$, $(i+k)^{th}$ row and the $(j\pm k)^{th}$ columns, for all the possible k until such an element is found.

The union of good elements in C_s and the assigned elements is called the selected set.

The fourth step in the algorithm imposes an order on the selected elements such that the mapping T, which is defined in the next sentence, is a topological isomorphism with its domain as the ideal array and its range as the elements of selected set.

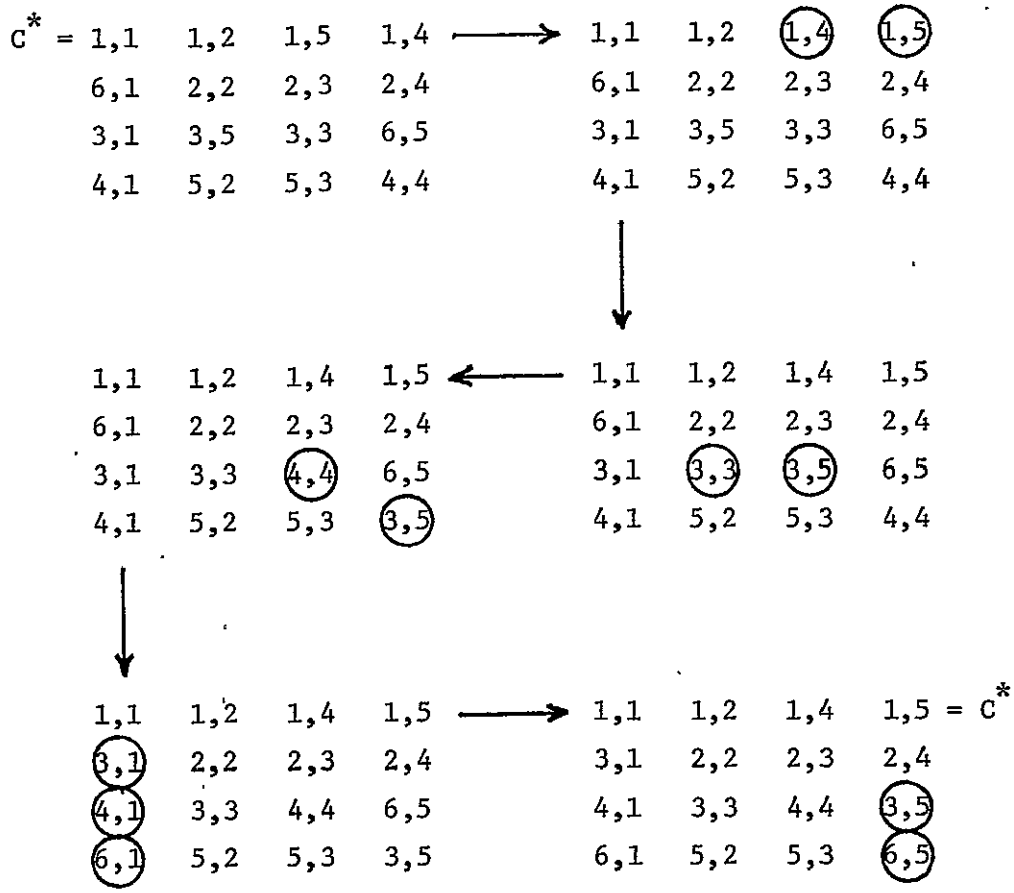
$$T : a_{ij} = C_{c^*_{ij}}$$

where

a_{ij} = an arbitrary element of ideal array.

$C_{c^*_{ij}}$ = a selected element of C whose indices are given by c^*_{ij}.

The elements of each row r of C^* are arranged from left to right in ascending order of the column index, j (see Fig. 3.11). The elements in each column k of C^* are arranged from top to bottom in



$$T: a_{ij} = c_{c^*_{ij}}$$

SELECT/SET - Step 4

Fig. 3.11

ascending order of row index, i. NOte that the individual elements and not just two indices are exchanged.

The following procedure is used in the case of equality between column indices of any two elements, say $c^*_{r,k}$ and $c^*_{r,k+1}$, of any row r in C^*. The $(k+1)^{th}$ column is searched for an element in exchange with $c^*_{r,k}$, which eliminates the equality. If no such element is available in column k+1, the k^{th} column is searched for a possible replacement for $c^*_{r,k+1}$. Similarly in the case of equality in row indices of two elements, $c^*_{r,k}$ and $c^*_{r+1,k}$, the $r+1^{th}$ and r^{th} row are searched for a possible replacement for $c^*_{r,k}$ or $c^*_{r+1,k}$.

This fourth step completes the selection and ordering of the useable set of elements.

INPUT TO THE PROGRAM

The program requires the data to be in free-form format and in the following order :

1. The first card must contain four integers: m, n, p and q, where:

m = number of rows of elements on the chip,

n = number of columns of elements on the chip,

p = number of rows of elements on ideal chip,

q = number of columns of elements on ideal chip.

2. The following m cards must contain c_{ij}'s in the following order:

C_{11}, C_{12}, --- ---, C_{1n},

C_{21}, C_{22}, --- ---, C_{2n},

--- --- --- --- ---

--- --- --- --- ---

C_{m1}, C_{m2}, --- --- C_{mn},

where : $c_{ij} = \begin{cases} 1 \text{ If the corresponding element on the chip is good.} \\ 0 \text{ If the corresponding element on the chip is bad.} \end{cases}$

OUTPUT OF THE PROGRAM

The program prints out a copy of the input chip representing each element by an integer, 1 if the element is good or 0 if the element is bad.

The indices of the arranged selected elements are printed in the form of an ideal array. A sample output is given in Fig. 3.12, while Fig. 3.13 has added to this solid lines connecting the row elements and dotted lines connecting the column elements so as to highlight the selected matrix. In this test case m=6, n=5, p=q=4.

CIRCUIT 2/ SIGNALS

This program determines the form of signal paths of a circuit. The circuit forms a 1-bit adder from a set of ten good NAND-gates. The NAND-gates connected by this program are those selected and suitably labeled by SELECT/SET. The circuit is described as various wire connections between different terminals of NAND-gates.

Hereafter the wire connections are called signals. The output consists of an array containing the end points and the path for each signal.

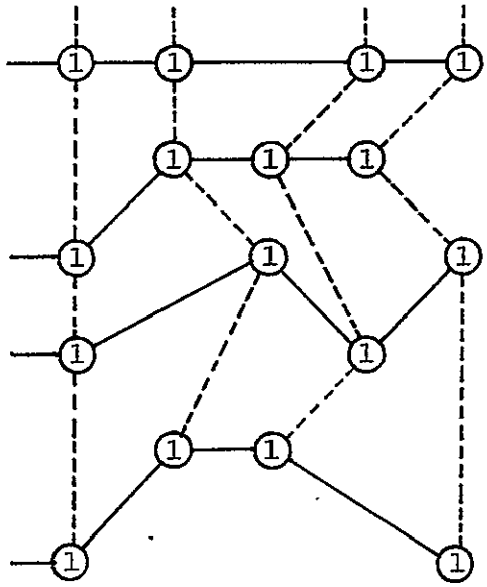
SAMPLE OUTPUT

```
1   1   0   1   1
0   1   1   1   0
1   0   1   0   1
1   0   0   1   0
0   1   1   0   0
1   0   0   0   1
1,  1   1,  2   1,  4   1,  5
3,  1   2,  2   2,  3   2,  4
4,  1   3,  3   4,  4   3,  5
6,  1   5,  2   5,  3   6,  5
```

SELECT/SET Output - The Selected Array

Fig. 3.12

SAMPLE RESULTS



SELECT/SET Output - Rows and Columns of Selected Array

Fig. 3.13

RESULTS

The program solved satisfactorily all the test cases. Some of the test cases are given below. In each case the nano-gates were taken to be in the form of an array on the chip. Size of the array varied from 4 x 4 to 4 x 6. Entries 1 or 0 represent a good or a bad nano gate respectively. The program connects the circled elements.

Test Case (1) (4 x 6 Array)

0	0	0	1	0	0
0	0	(1)	(1)	(1)	0
0	(1)	(1)	(1)	(1)	0
(1)	(1)	0	0	(1)	1

Test Case (2) (4 x 6 Array)

0	(1)	1	(1)	0	0
0	1	1	0	0	0
(1)	(1)	(1)	(1)	1	0
1	1	1	1	0	0

Test Case (3) (4 x 5 Array)

1	(1)	0	0	0
(1)	0	0	0	(1)
(1)	(1)	0	(1)	(1)
0	(1)	(1)	(1)	0

Test Case (4) (4 x 5 Array)

0	(1)	(1)	(1)	0
0	(1)	0	(1)	(1)
1	0	(1)	(1)	(1)
1	(1)	0	0	0

Test Case (5) (4 x 4 Array)

(1)	(1)	0	0
(1)	0	(1)	(1)
0	(1)	0	(1)
0	(1)	(1)	(1)

Test Case (6) (4 x 4 Array)

0	(1)	0	(1)
(1)	0	(1)	(1)
(1)	(1)	0	(1)
1	(1)	(1)	0

The results of this program have been successfully used by the program TRANSLATE/SIGNALS. An example of results is shown in Fig. 3.14.

2

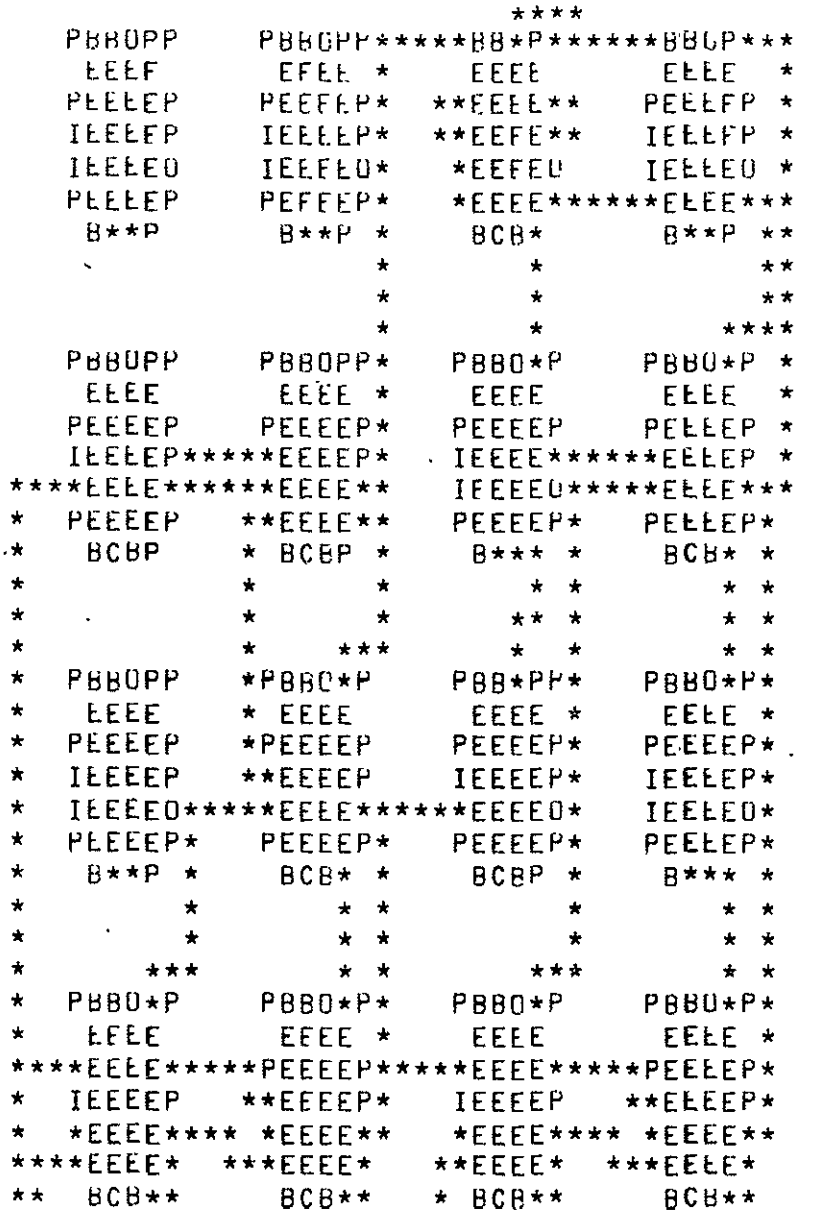


Fig. 3.14 Circuit 2/signals - typical output

GENERAL DISCUSSION

The circuit as described for an ideal array (see Fig. 3.15) consists of a subcircuit (inside the dotted line) repeated two times. The second time the relative position of the originating point of input signals and the termination point of output signals is different.

The complete circuit is described by individual signals. Each signal is described by a combination of alternate moves in the horizontal and vertical directions. The description of a signal s is stored in the s^{th} row of a two dimensional array. The entries in a row of the array are selected as follows. The first entry indicates whether the direction of a move is horizontal or vertical. The following two entries are x and y coordinate of the originating point of the signal. Since each move is normal to the preceding one, it is sufficient to give only one coordinate for each corner. Therefore the entries following the coordinates of the originating point are the x or y coordinate of each corner in sequence.

ALGORITHM

The first step in describing a circuit on a chip is to represent the chip by a two dimensional array R which is called the representation array. The array R represents each element on the chip with its terminals, the available space for the wires and the input output terminals. For example, in the test cases there was a space for four wires between any two gates and each gate had three horizontal and a vertical pass, two input terminals, two output terminals, two bus lines and a disable terminal, to be connected to the ground bus in case the element was not used in the circuit. Each gate was represented by

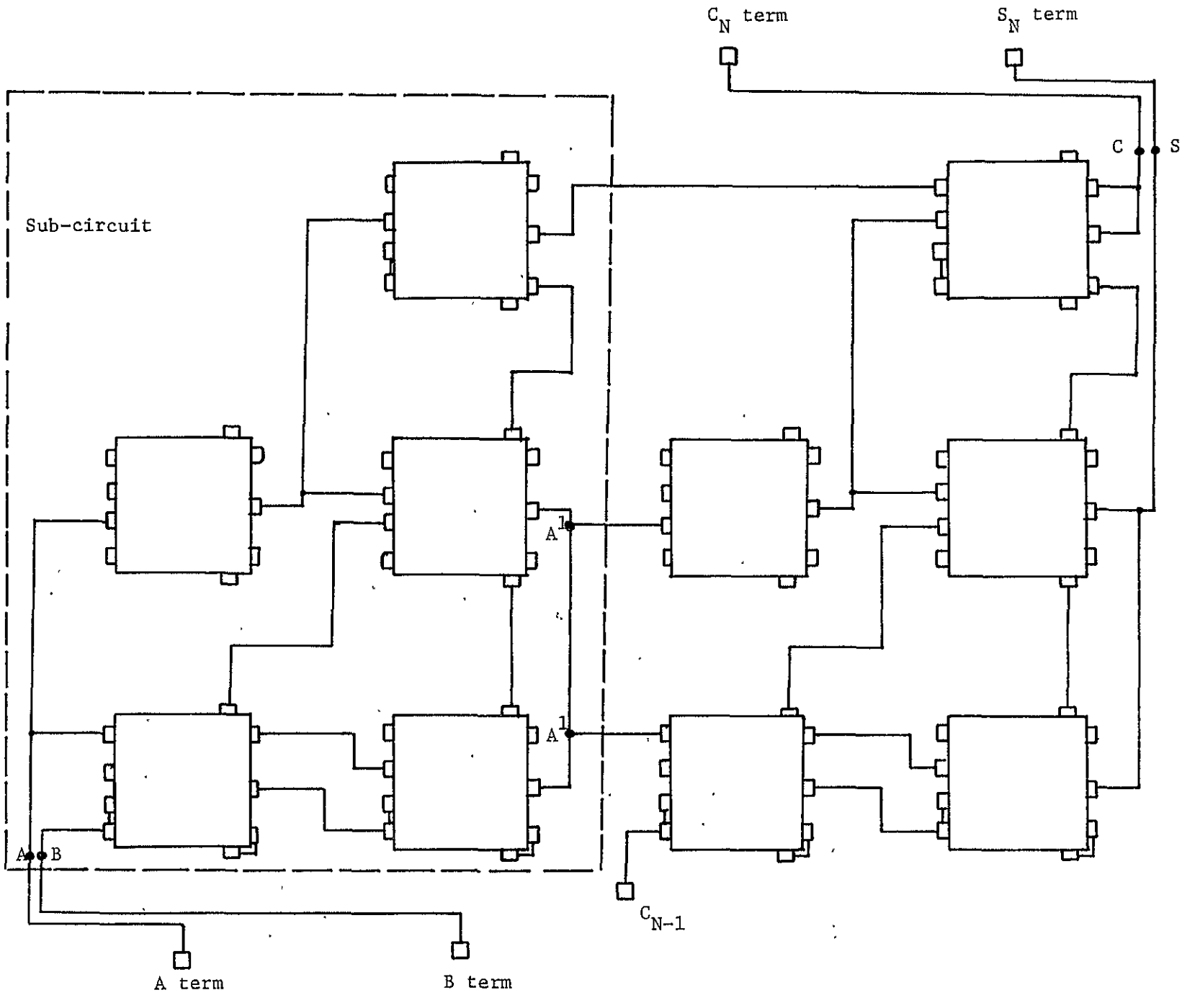


Fig. 3.15 Circuit for ideal 10-gate array

```
        B   B   O   P
    P   E   E   E   E   P
    P   E   E   E   E   P
    I   E   E   E   E   P
    I   E   E   E   E   O
    P   E   E   E   E   P
        B   C   B   P
```

where O's are the output terminals, I's are the input terminals, B's are the power bus terminals, P's are the pass (undercrossing) terminals and the C is the disable terminal of the gate. This corresponds to the gate layout represented schematically in Fig. 3.16.

The complete circuit is described by first connecting the input terminals AT and BT to the points A and B respectively (see Fig. 3.15) and the output terminals CT and ST to the points C and S respectively. Then the subcircuit is described on the first set of five gates using the points A and B as the originating points for the input signals. After having described the subcircuit on the first set, the position of the inputs for the second set are determined (marked as A' and B' in Fig. 3.15) and the desired paths are drawn to bring them to suitable points for the next set. Now the subcircuit is described on the second set of five gates using these points as the originating points for the input signals. Finally the outputs of the second set are connected to the points S and C and all the unused gates are disabled.

The signals are described with respect to the coordinate system with its origin at R[0,0]. Y axis is considered positive downward.

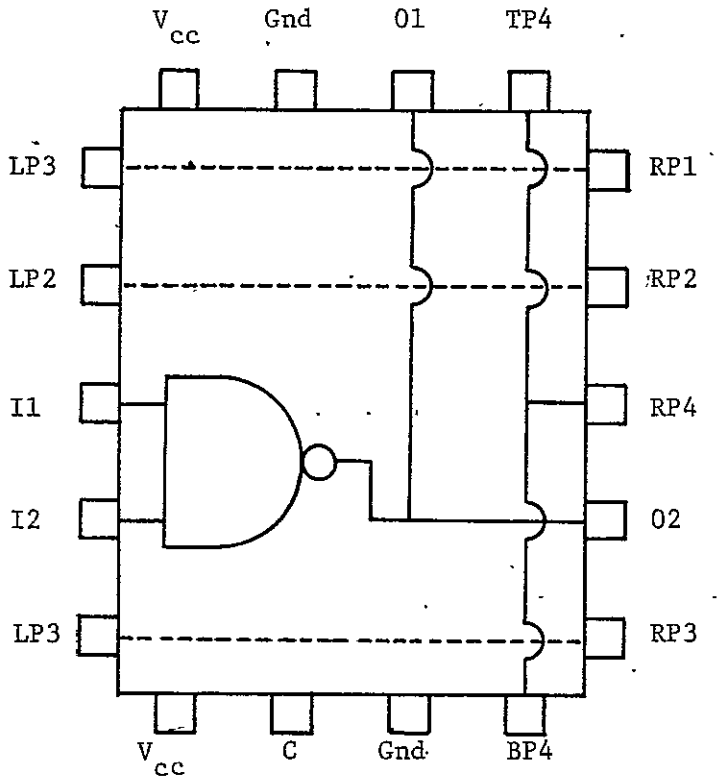


Fig. 3.16 Gate schematic

The X axis is positive to the right. When a description of a signal is completed, its path in R, the representation array, is shown by *'s (see Fig. 3.14).

DESCRIPTION OF SUBCIRCUIT

Let G_1, G_2, G_3, G_4, and G_5 be a set of gates. Let the input A be the line connecting (XO, YO, and (XO, YM), (note that YO can be the same as YM) and the input B be at the point XB, YB. Let LP1, LP2 and LP3 be the left end and RP1, RP2, RP3 be the right end of the upper, middle and lower passes of each gate (see 3.16). Let I_1 and I_2 be the two input terminals and 01 and 02 be the output terminals. Finally let BP4, RP4 and TP4 be respectively the bottom, the right and the top end of the vertical pass in the gate.

The description of the sub-circuit is started at the upper left corner, taking one signal at a time, and the description continues towards the lower right corner. Wherever possible, the description of a signal is started at its left end point.

The subcircuit is described in three mian procedures. In the first procedure the following signals are drawn.

Input A is connected to I2 of G_1. 01 of G_1 is connected to I1 of G_3 and to I1 of G_4 in two parts. The first part describes signal(s) to connect 01 of G_1 to I1 of G_3 and the second part describes another signal(s) to connect this signal with I1 of G_4.

Next in the series we draw a signal(s) to connect an output (01 or 02) of G_3 with LP1 of the last gate in the first row on the chip. Last signal(s) in this procedure connects TP4 of G_4 to I2 of G_3.

The second procedure describes the signals connecting the gate G_2 with the input terminals and the gates G_4 and G_5.

The input A and B are connected respectively to the LP2 and LP3 of G_2. Then LP3 and J2 of G2 are connected to each other. We connect the RP3 and BP4 of G_2 to each other and then the TP4 is connected to I_2 of G_4.

Next in series we connect RP2 and 02 of G_2 respectively to I1 and LP3 of G_5. The last signal in this procedure connects I2 and LP3 of G_5.

The third procedure describes the signals between G_4 and G_5.

First the TP4 of G_5 is connected to the BP4 of G_4, and then 02 of G_4 is connected to 02 of G_5. Lastly the RP3 and the BP4 of G_5 are connected to each other.

In a precisely parallel manner, the second subcircuit is intraconnected to complete the one-bit adder configuration. The computer program TRANSLATE/SIGNALS was developed to interpret the wire routing results of CIRCUIT/SIGNALS into an input format appropriate to the SEMTAPE/COMPILE program described in Section 4.2 below which converts geometry specifications into a control magnetic tape for the EMG. TRANSLATE/SIGNALS converts the signal path description and coordinates from the abbreviated path description and reduced coordinate system used in CIRCUIT/SIGNALS into the five-number rectangle description required by SEMTAPE/COMPILE and the coordinates corresponding to points on the actual circuit chip.

Test cases were prepared for exercising these programs to develop the final circuit configuration for the one-bit adder, using 10

gates from a 4 x 4 gate array, and assuming 2, 3, 4, 5, and 6 bad gates per array. The test case inputs and outputs for these five classes of problem are shown in Figs. 3.17 through 3.21. CRT presentations of several of the resulting EMG patterns are shown in Figs. 3.22 and 3.23. Photographs of the actual metal patterns on a chip are presented in Section 5.1 below.

THE INPUT MATRIX IS

1 1 1 1

0 1 1 1

1 0 1 1

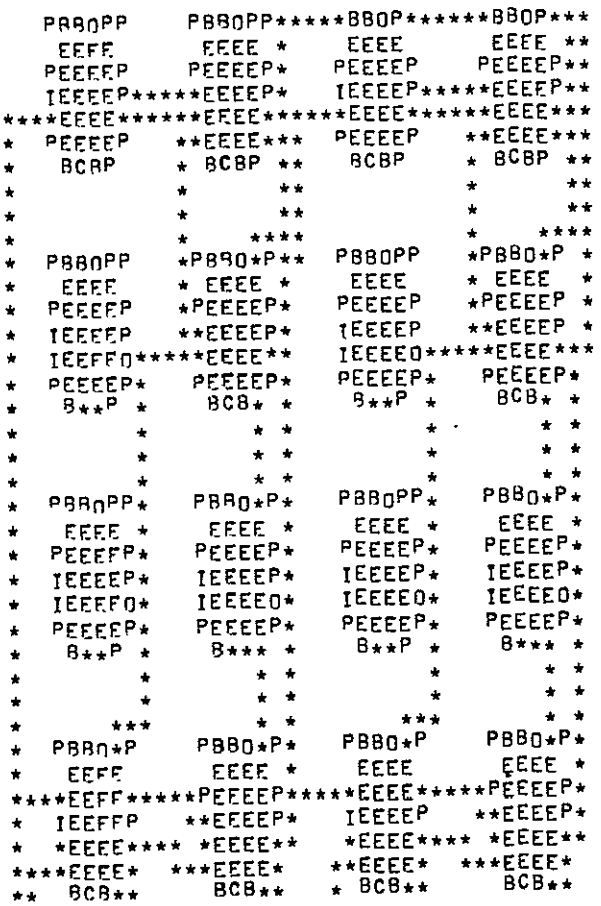
1 1 1 1

SELECTED SET OF ELEMENTS IS

0, 0 1, 2 0, 0 1, 4

1, 1 2, 2 1, 3 2, 4

4, 1 4, 2 4, 3 4, 4



Case 201

THE INPUT MATRIX IS

0 1 0 1

1 1 1 1

1 1 1 1

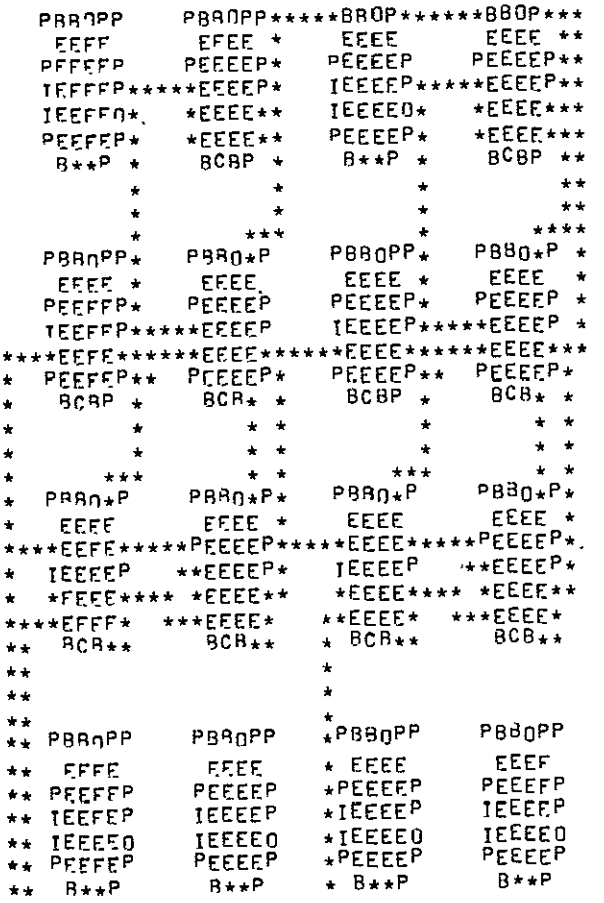
1 1 1 1

SELECTED SET OF ELEMENTS IS

0, 0 1, 2 0, 0 1, 4

2, 1 2, 2 2, 3 2, 4

3, 1 3, 2 3, 3 3, 4



Case 202

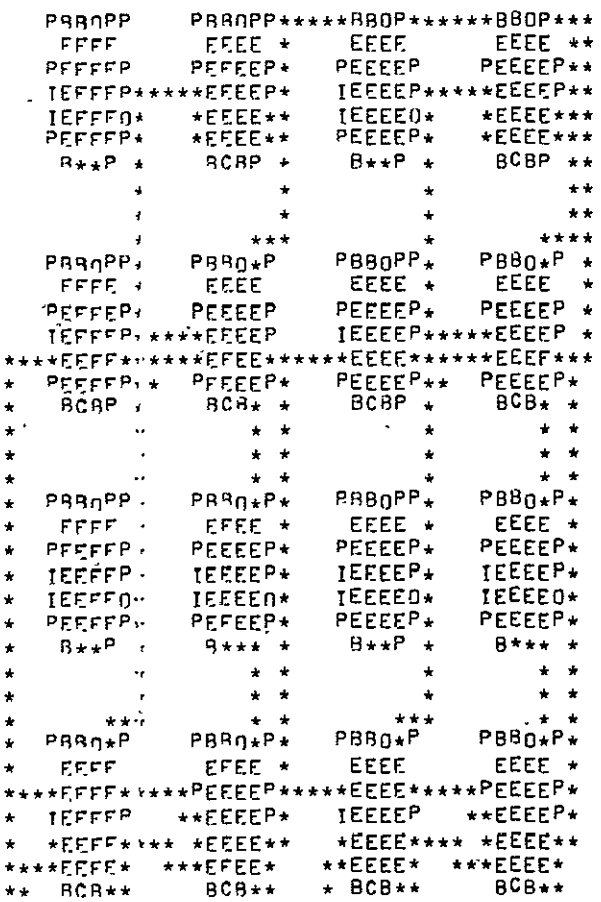
Fig. 3.17 Test Cases with 2 Bad Gates

THE INPUT MATRIX IS

0	1	0	1
1	1	1	1
1	0	1	1
1	1	1	1

SELECTED SET OF ELEMENTS IS

0,	0	1,	2	0,	0	1,	4
2,	1	2,	2	2,	3	2,	4
4,	1	4,	2	4,	3	4,	4



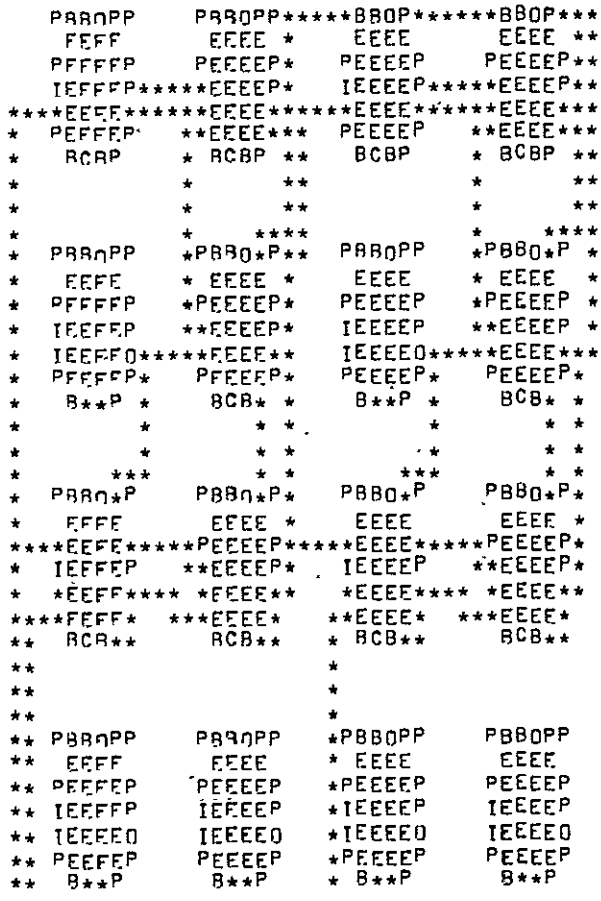
Case 301

THE INPUT MATRIX IS

1	1	1	1
0	1	1	1
1	1	1	1
1	0	0	1

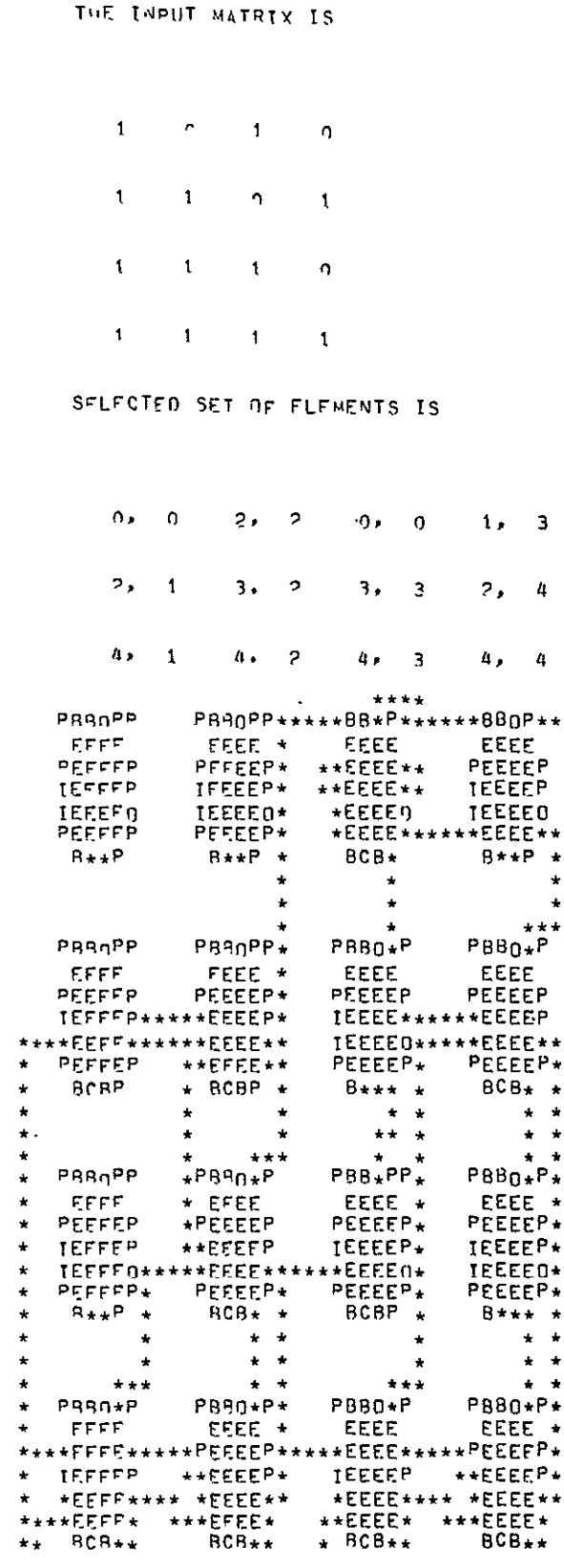
SELECTED SET OF ELEMENTS IS

0,	0	1,	2	0,	0	1,	4
1,	1	2,	2	1,	3	2,	4
3,	1	3,	2	3,	3	3,	4



Case 302

Fig. 3.18 Test Cases with 3 Bad Gates



Case 401 Case 402

Fig. 3.19 Test Cases with 4 Bad Gates

THE INPUT MATRIX IS

1 0 1 1

1 1 0 0

0 1 1 1

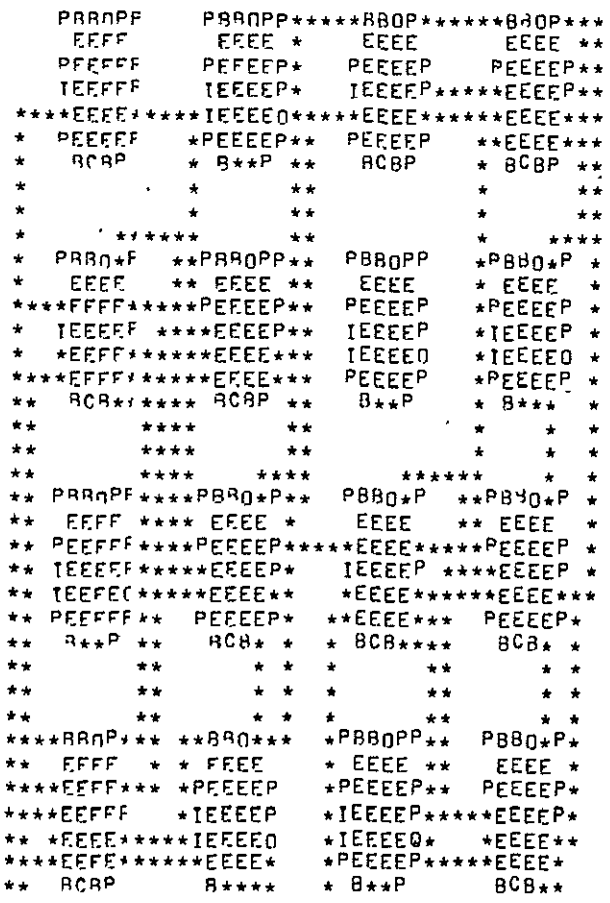
1 0 1 1

SELECTED SET OF ELEMENTS IS

0, 0 2, 2 0, 0 1, 4

1, 1 3, 2 1, 3 3, 4

2, 1 4, 1 3, 3 4, 4



Case 501

THE INPUT MATRIX IS

1 1 1 0

0 1 1 1

1 0 1 0

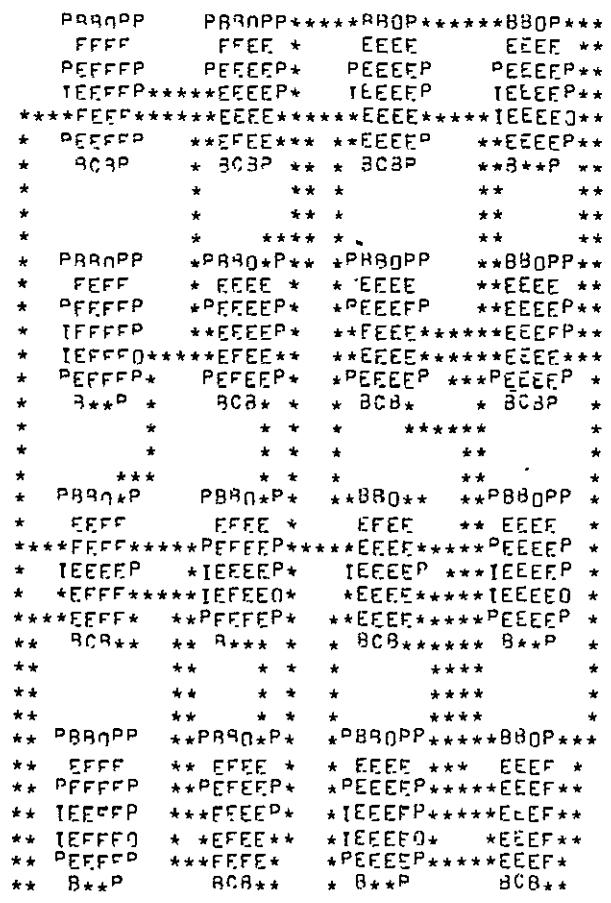
1 1 0 1

SELECTED SET OF ELEMENTS IS

0, 0 1, 2 0, 0 2, 4

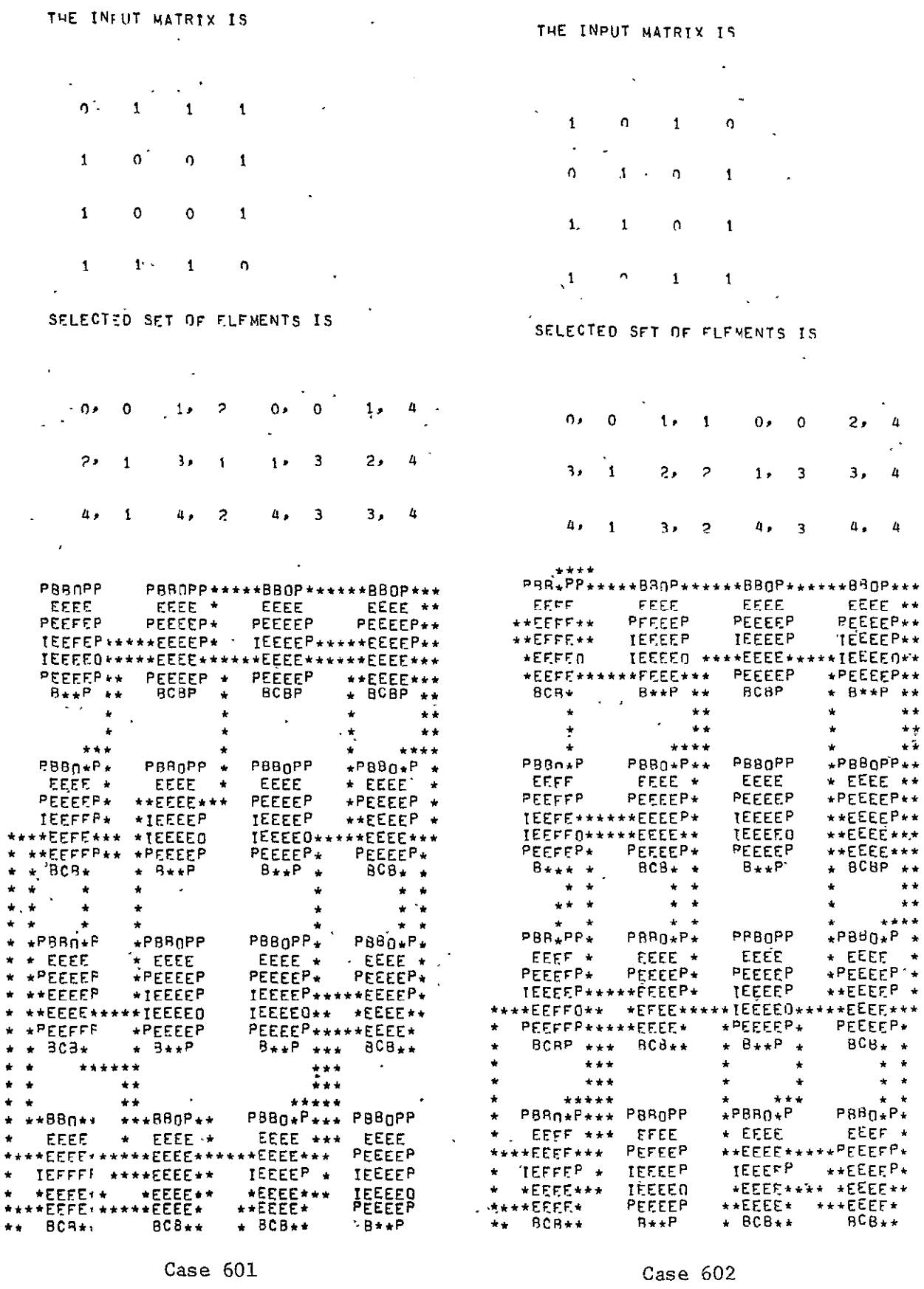
1, 1 2, 2 1, 3 2, 3

3, 1 4, 2 3, 3 4, 4



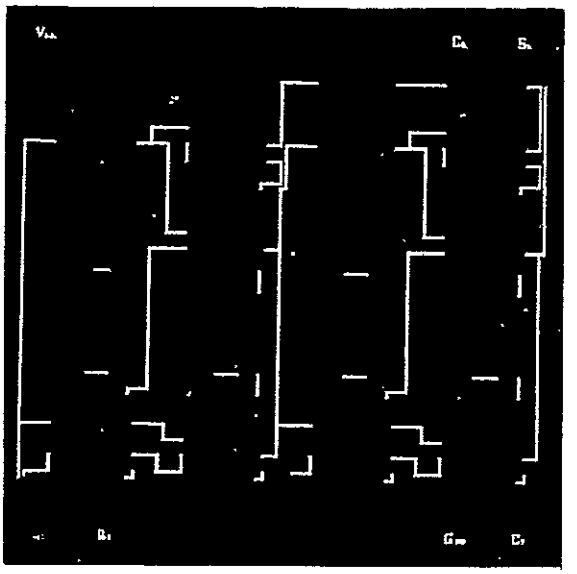
Case 502

Fig. 3.20 Test Cases with 5 Bad Gates

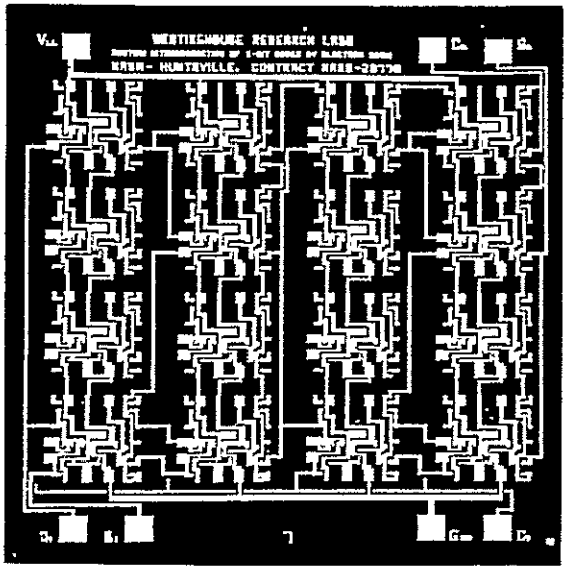


Case 601 Case 602

Fig. 3.21 Test Cases with 6 Bad Gates

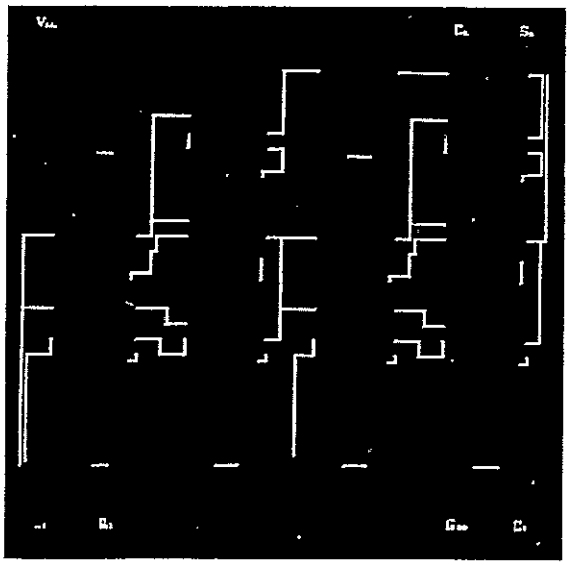


Second Metal

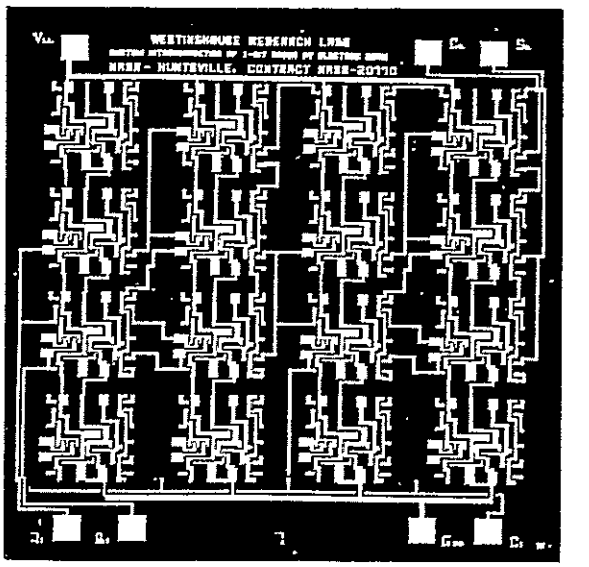


First and Second Metal

Case 201



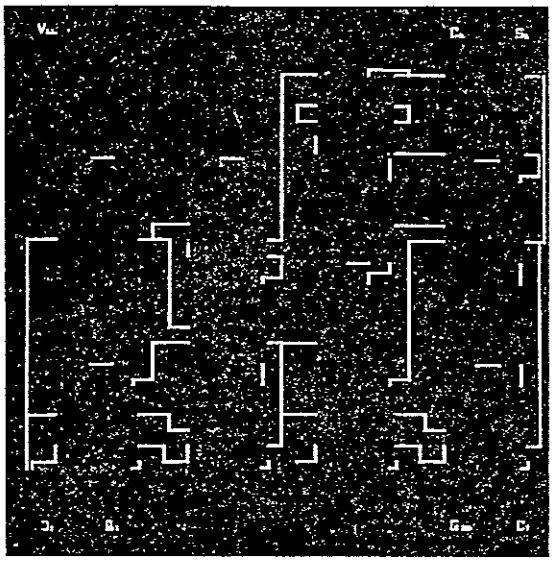
Second Metal



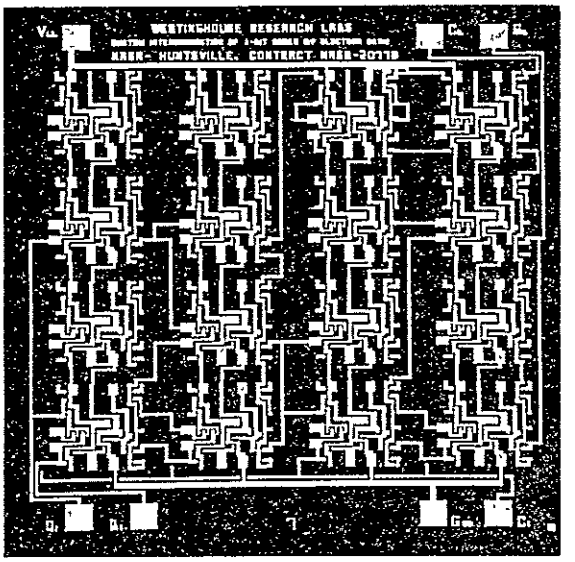
First and Second Metal

Case 202

Fig. 3.22 - Test Cases - Wiring Patterns

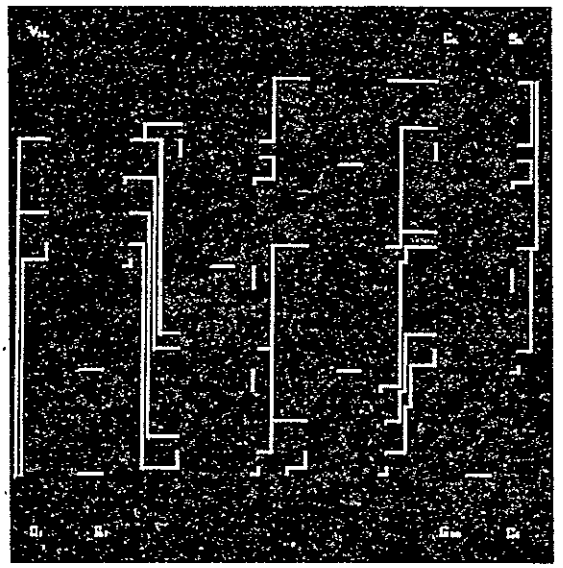


Second Metal

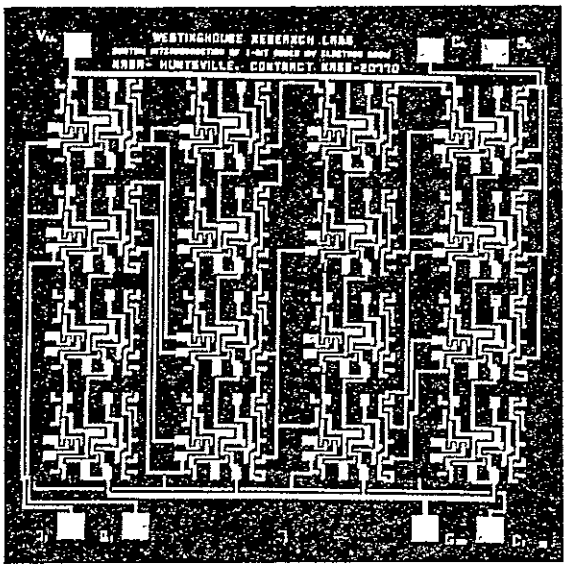


First and Second Metal

Case 401



Second Metal



First and Second Metal

Case 402

Fig. 3.23 - Test Cases - Wiring Patterns (Continued)

4.0 ELECTRON BEAM SYSTEMS DEVELOPMENT

Electron beam systems and their application to the fabrication of solid-state devices have been under study at Westinghouse Research for about 10 years, and as a result, two apparatuses have been developed for use in defining device geometries, namely, the computer controlled scanning electron microscope, now referred to as the Electron Micropattern Generator, and the Electron Image Projection System, which uses a high intensity image tube. In the present program, only the Electron Micropattern Generator was used as a fabrication tool, and much of the effort was devoted to developing and perfecting this system and the computer programs which control it. At the start of the program, the digital control for the scanning electron microscope had been planned and partly assembled, but it was not until several months after the start of the program until the first patterns were produced under computer control. The following paragraphs describe some of the aspects of this development including hardware design and improvement, software development, alignment techniques, and system capabilities.

4.1 ELECTRON MICROPATTERN GENERATOR (EMG)

The Electron Micropattern Generator (EMG) used in this program is built around a scanning electron microscope designed and constructed at Westinghouse Research in 1962 by O. C. Wells. As shown in Fig. 4.1, the apparatus includes the electron beam column with its gun, condensing and objective lenses, scanning coils, sample chamber, and vacuum system. Both an analog control for using this in the conventional manner as a microscope, shown at center, and a digital control employing magnetic

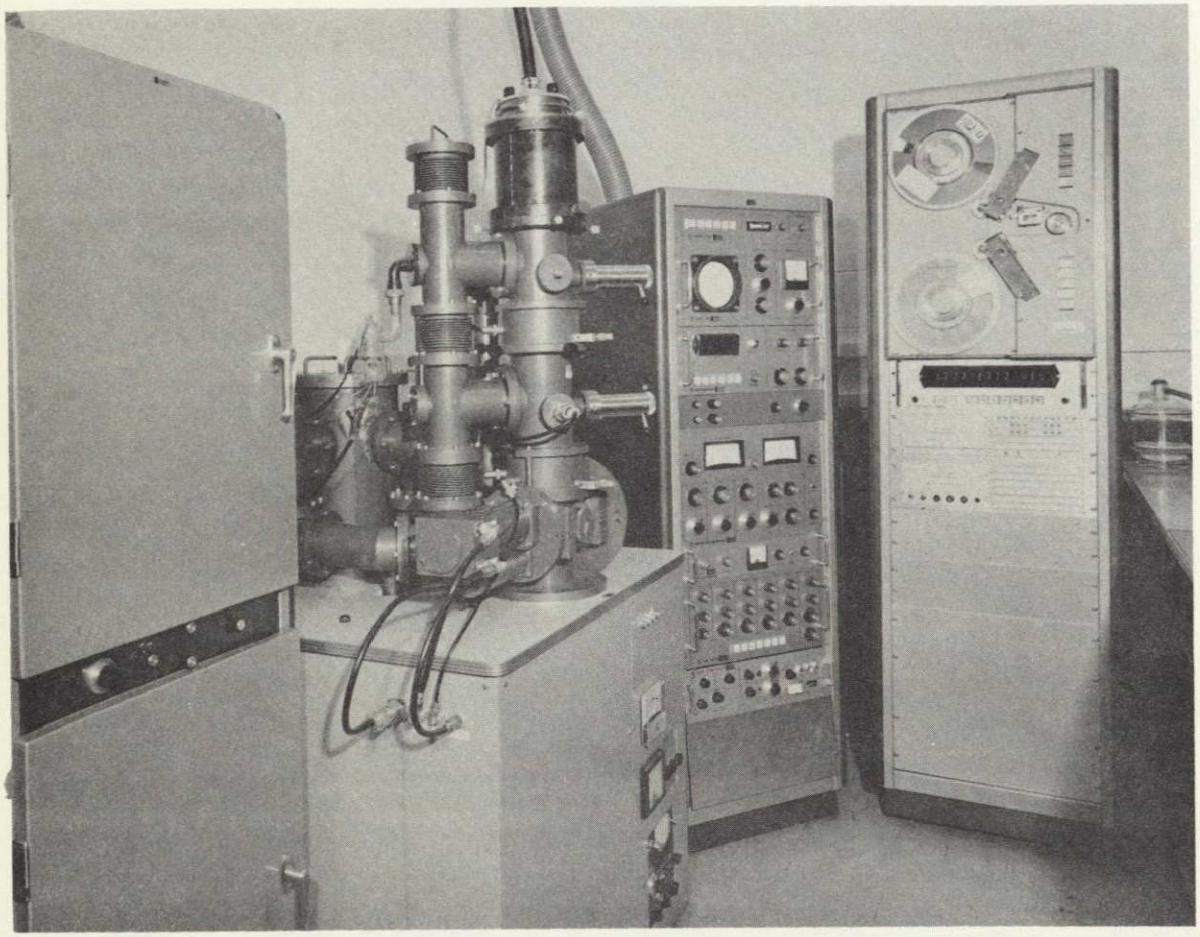


Figure 4.1 -- Electron Micropattern Generator

tape as an information transfer medium, shown at the right, are used with the column.

It was decided very early in the design period to use the Burroughs-5500 digital computer to perform as much of the over-all task as possible, and to use magnetic tape as a transfer medium for data inputting into the digital control hardware. Objectives of high accuracy and fast operating speeds served as a guide to the system design. A 36 in. per second Ampex Type TM-71DH tape transport was selected for the data input terminal, and further design considerations were dependent, in part, on the specifications and characteristics of this drive. Selection of the operating field-of-view of the microscope was influenced by factors such as effective beam width, column and deflection system stability, pattern complexity, and desirable beam addressing rates. A 4092-address X and 4096-address Y field with a 1/2 micron basic increment of distance was chosen as a suitable compromise of these criteria, giving an operating field 2045.5 x 2047.5 microns in size, or approximately 80 by 80 mils. A further objective of the design was to provide for numerous machine functions so as to lead ultimately to a completely automated unit. The presently used machine functions, as well as those provided for future use, are listed in Table 4.1.

This system permits the exposure of arbitrary desired patterns on electroresist covered targets and eliminates the need for any preparation of scale drawings, art work, photographic masters, or any of the photolithographic steps commonly employed in today's integrated circuit technology.

Present:

1. Beam Position
2. Beam On/Off
3. Program Serial Number
4. Word Rate
5. End of Program
6. Set MSB and NMSB

Future:

1. Subscan Specification
2. Digital Stage Position
3. Electronic Alignment Instructions
4. Electron Beam Testing Instructions

EMG Machine Functions

Table 4.1

DESIGN AND OPERATION

The digital control rack, shown at the right of Fig. 4.1 houses at the top the Ampex tape deck, next the main chassis of the EMG digital control, and beneath that the magnetic core memory unit which serves as a buffer between the tape deck and the word register in the digital control. The overall flow of data in this system is shown in Fig. 4.2. Inputs to the Burroughs-5500 computer consist of the appropriate software programs such as the SEMTAPE/COMPILE program stored on discs, and geometry specifications in digital form inputted in punched

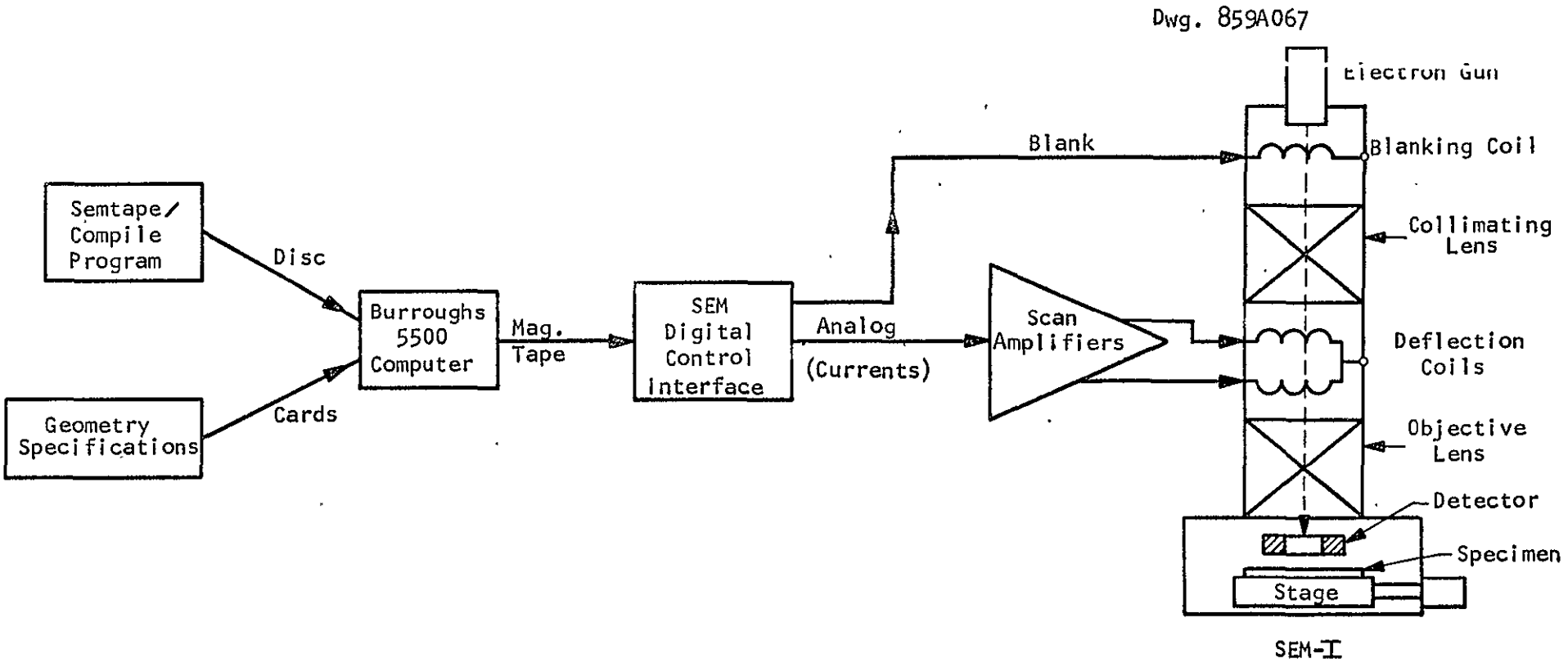


Fig. 4.2 EMG data flow

card format. Using these inputs, the Burroughs computer outputs a 2400 ft. reel of 7-track magnetic tape which has the machine control information on it. The digital control interface then manipulates and interprets the incoming data from the tape and executes machine functions as they occur. Most of the data are beam addresses and serve to control the scan amplifiers which drive the deflection coils.

The EMG digital control operates with a four-character word as shown in Fig. 4.3. In each of the four characters, five bits serve as data bits, while the sixth bit serves as a word mark location. As the characters are loaded into the control word register, the first character carries the first low order digits of the X address portion of the word, the second character carries the last five digits of the X address, and similarly for the third and fourth characters for the Y address. X^6, X^{12}, and Y^6 are word mark digits in the first three characters and have the value of 0. Y^{12}, on the other hand, in the fourth character serves a word mark and has the value of 1. As written on the magnetic tape by the Burroughs computer, the data characters which form the EMG digital control word are listed in records which are 2048 characters in length. This record length was chosen so as to be compatible with the 4096 character capacity of the magnetic core memory which serves as a buffer. The core memory is of sequential interlace design, which permits writing characters in it in numerical sequence and reading characters out of it in a separate numerical sequence. Read and write address registers in the core memory count from 0 to 4095 in a 12-bit binary counter, and electrical flags or signals made

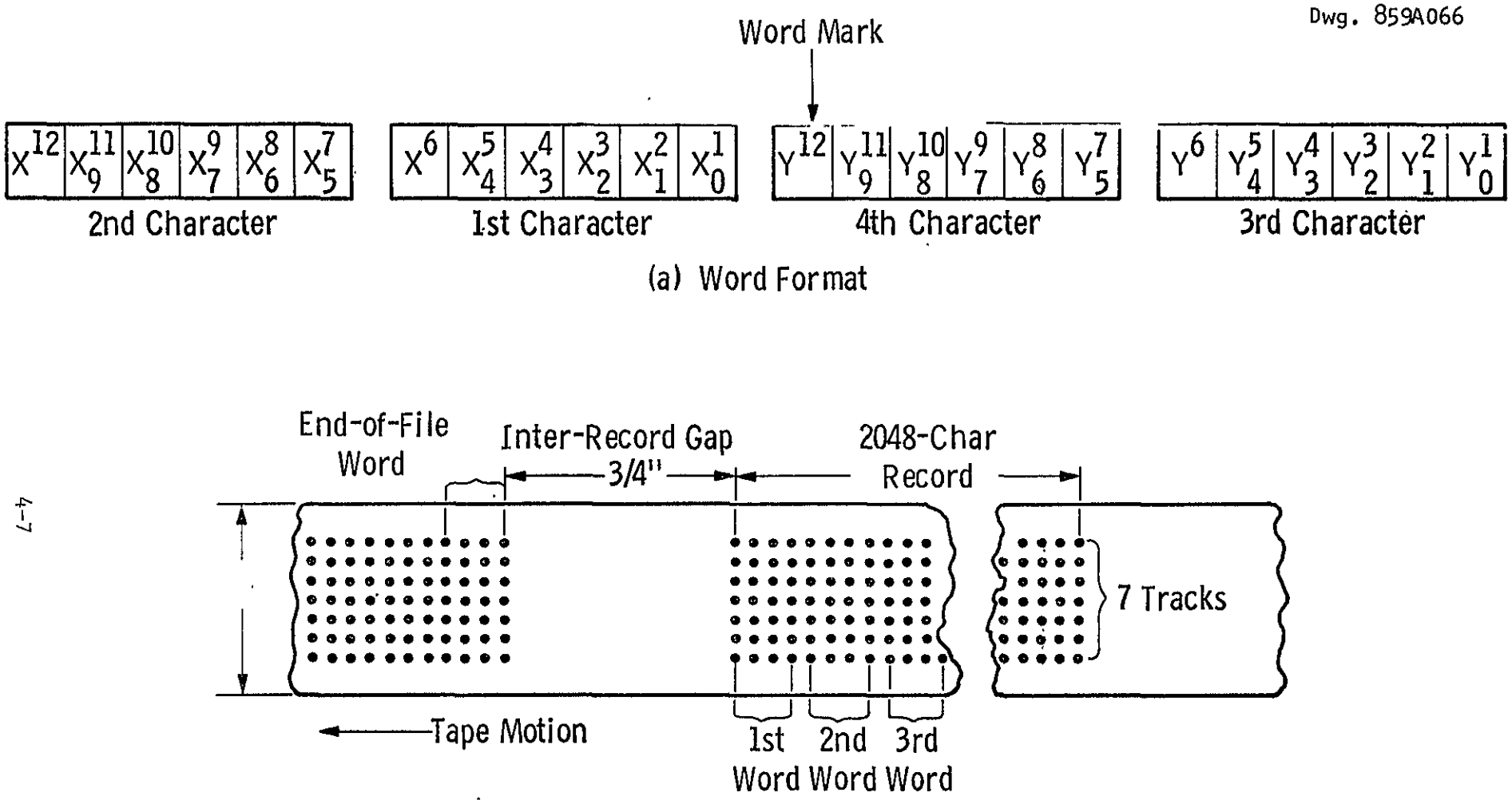


Fig. 4.3 Format for EMG digital control data

available on the eleventh bit of this counter signal when the counter has reached one-half of full capacity count. These flags or signals are used by the EMG digital control to monitor the load/unload status of the core memory. They also permit refreshing one-half of the capacity of the core memory at a time by reading a new record of 2048 from the tape and then writing that record into the newly unloaded core. In operation, the EMG control is started by manual controls and the characters that are stored in the core memory are read into the interface in a continuous stream; meanwhile, the tape reader reads in 2048-character increments until it reaches the end-of-file. The end-of-file is marked by a special machine function word, and signifies completion of that part of the pattern. To initiate a new or following pattern, the EMG digital control must be reactivated by the Start pushbutton.

The over-all organization of the EMG is shown in Fig. 4.4. The digital control is exercised primarily by the EMG digital control main chassis shown in the center of this figure, which handles all timing, assembles the characters into a machine word in a word register, detects, interprets and executes machine functions, converts address words into analog currents which ultimately control the deflection coils of the column, and permits manual control of the over-all operation. The Function Control panel shown at the lower left of the figure serves to switch the scanning electron microscope from an analog mode to an align mode or to a digital mode operation, permits adjustment of the alignment display, which is presented on a Tektronix Type 561 oscilloscope, and permits manual adjustment of the subscan size.

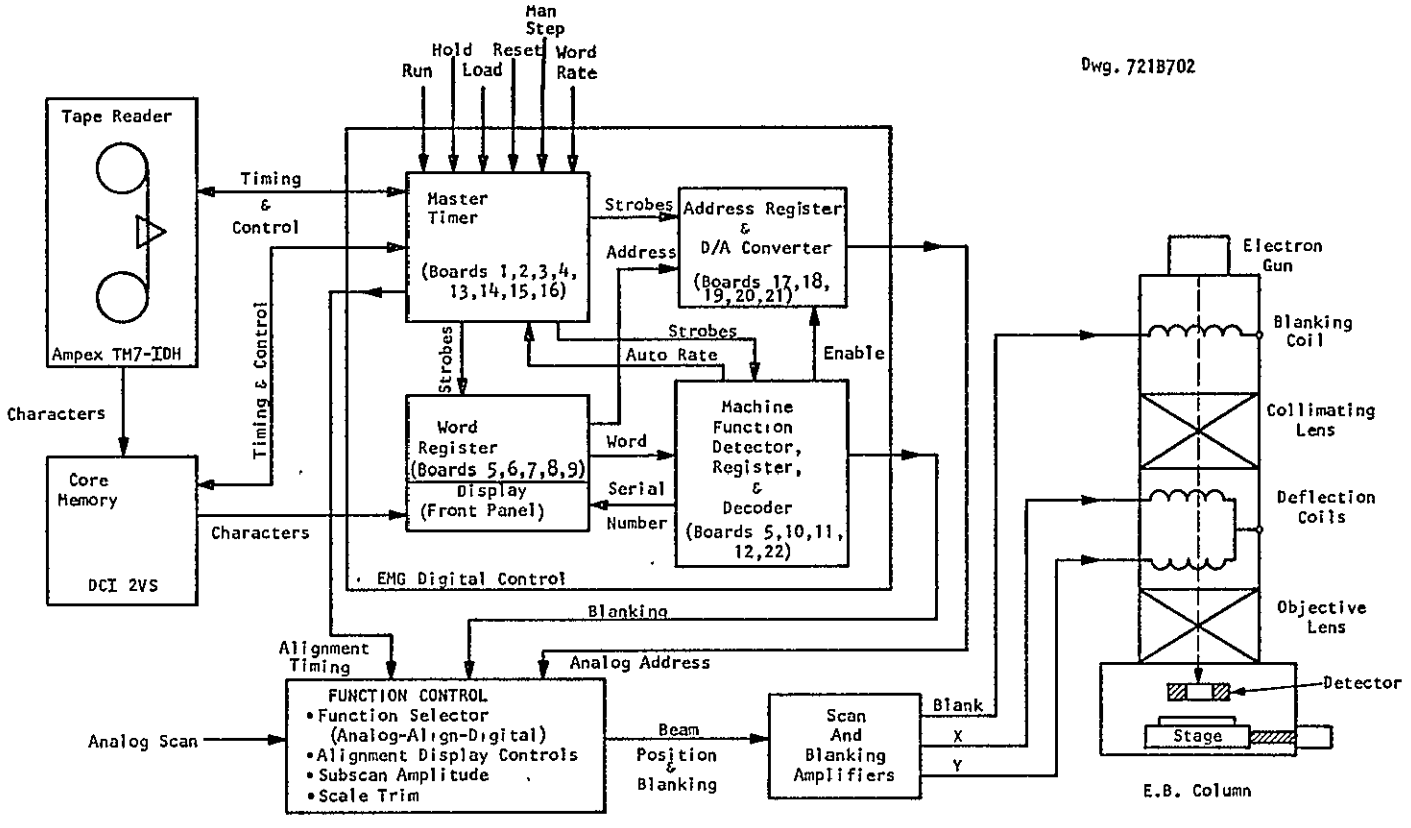


Fig. 4.4 Function diagram of Electron Micropattern Generator

The control is an all-solid-state design employing both integrated circuits and discrete components to perform the various functions. A photograph of this unit is shown in Fig. 4.5 while Fig. 4.6 shows the chassis layout. The 300 active components, roughly equally divided among logic gates, transistors, flip-flops, and operational amplifiers, are mounted on 22 plug-in type circuit boards. The front control panel presents displays of the X and Y address register contents, the program serial number obtained from a machine function word, and the word rate, which may be controlled either manually or automatically as directed by a machine function word. Aside from the word selector switch and the display intensity control, all operations are controlled by simple push-buttons. The operator steps required for reading a fabrication program into the EMG are extremely simple and consist of only four operations once the equipment has been turned on and the necessary column alignment obtained. These four steps are:

1. Tape deck controls are set to Remote, High Density, and Continuous.
2. The EMG Reset button is depressed to prepare for initial load.
3. The Load button is depressed twice to fill the buffer with two data records or blocks before start of exposure.
4. The Run button is depressed. This starts the feeding of information from the buffer store to the EMG control at the selected rate, and lights the Run indicator. At the end of the program, the information flow stops and the Run lamp goes out. The program serial number is displayed at the beginning of this program run and held until the beginning of the succeeding run.

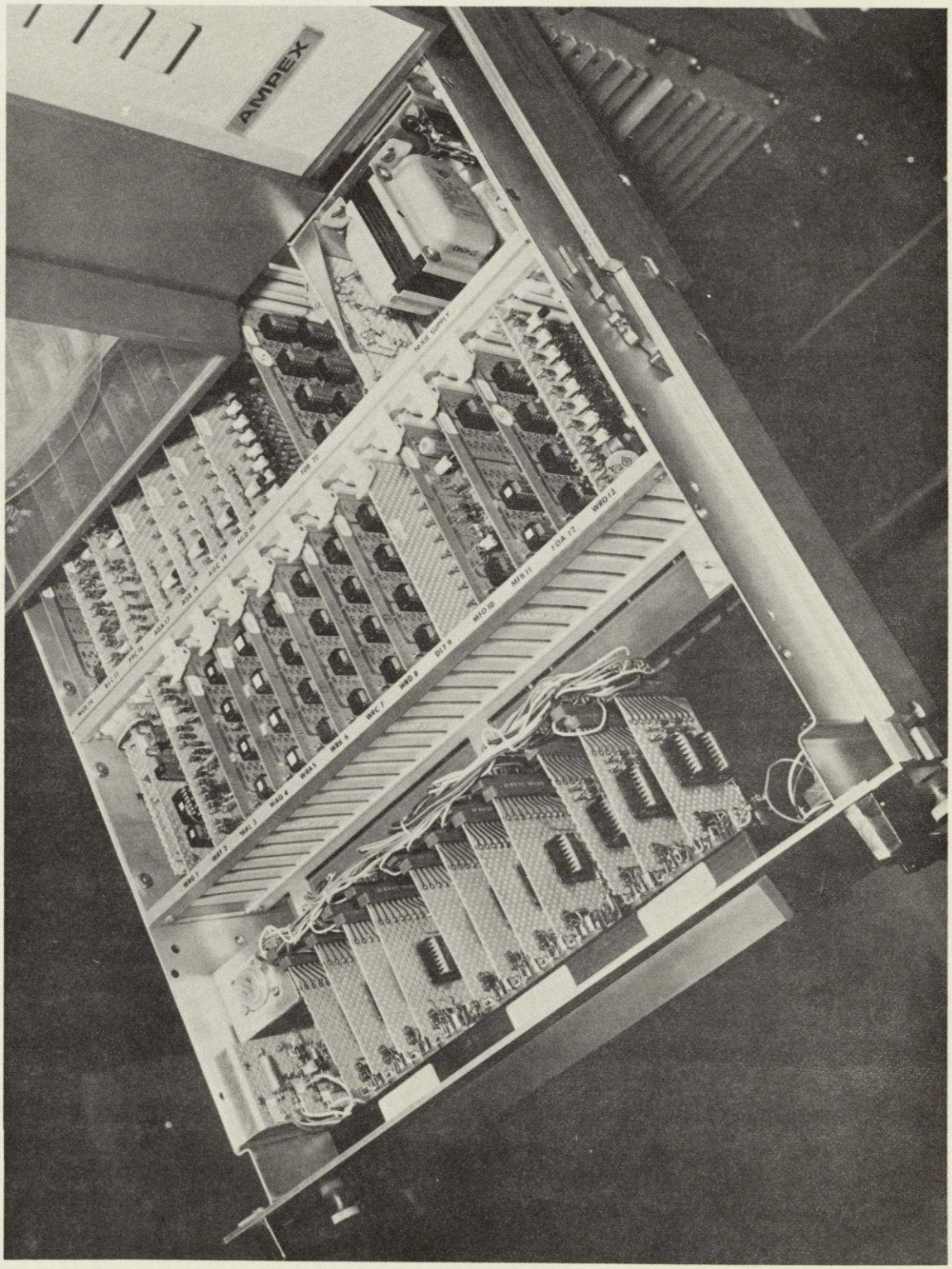


Figure 4.5 -- EMG digital control

Dwg. 859A069

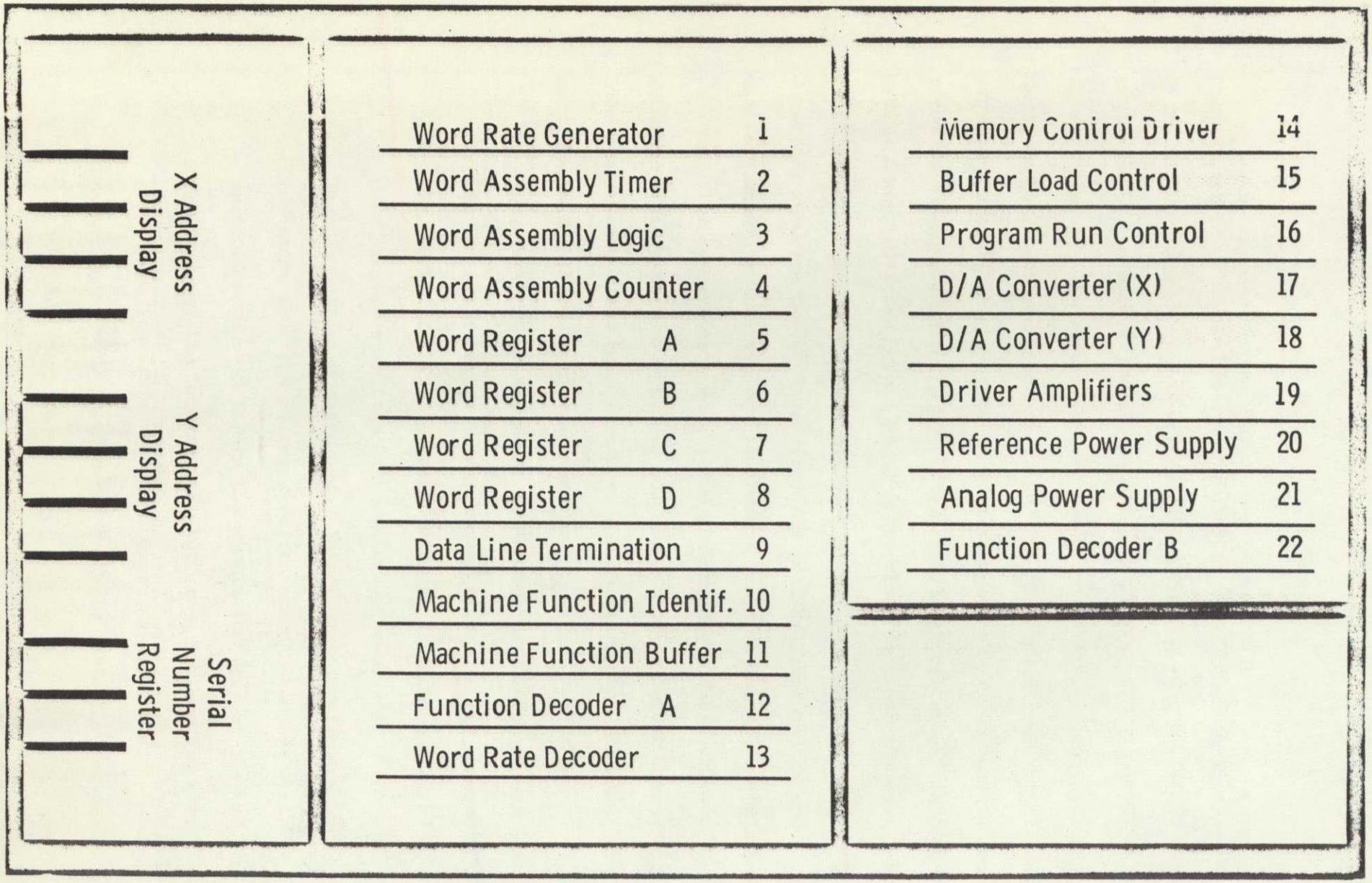


Fig. 4.6 Chassis layout of EMG digital control

In aligning successive patterns with the EMG, the function selector is switched to the align position, and a magnified image of a pre-selected alignment mark is displayed on an oscilloscope. At the same time, a digital pattern of a corresponding alignment frame which has been stored in the core memory and is recirculated there is superimposed on the alignment mark display. Suitable positioning controls permit adjusting the pattern positions so that exact alignment is obtained. A typical alignment mark and frame presentation is shown in Fig. 4.7

A continuing program to develop and refine the EMG and its operation has been in effect during this contract, and the more significant of the many improvements made are listed in Table 4.2.

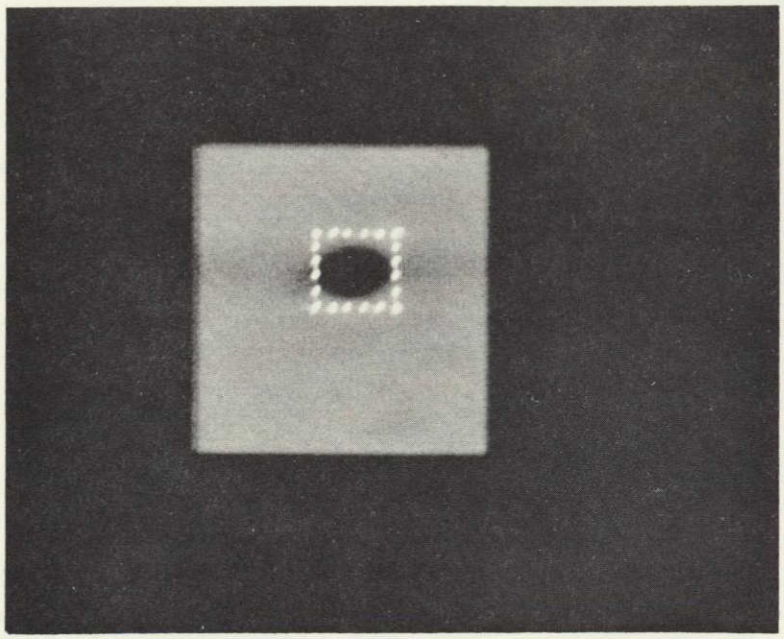


Figure 4.7 -- EMG alignment mark and digital frame (Scale 1 cm. - 2.5μ)

Table 4.2

Steps in Development and Improvement of the Electron Micropattern Generator

Problem	Solution or Modification
Basic Inadequacy of D/A Converter	Installation of new D/A converter with separate portable power supply for remote calibration
Need of 4096-point X and Y address	Change of machine design and software to accommodate 12-bit X and Y addresses, using machine function to set MSB and NMSB digits
Inadequate range and stability of pattern position control	Installation of new high resolution positioning control and stable operational amplifiers; increase of feedback ratio of scan amplifier 5X, installation of stable input amplifier and current sampling resistors.
A.F. and R.F. noise on deflection signals	Installation of shielding on scan amplifiers, revising of grounding system, change of deflection amplifier from voltage feedback to current feedback configuration with input summing junction. Installation of Paraformer line conditioner to reduce noise from line. Installation of separate power supplies for the control chassis and analog system.
SEM column instability with sample chamber	Provision of vacuum valves between sample chamber and column. Change of operation routine to eliminate gas bursts which destroyed filament through heavy discharges. Changeover to commercial filament for gun.
Excessive Digital Beam Addresses Per Pattern	Provision of manually selected subscan with 1, 2, 3, 4 and 5 micron square patterns.
Inadequate Alignment Procedure	Provision of alignment system and control with SEM display of restricted, manually positioned scanned raster and oscilloscope display of composite registration patterns.
Poor Alignment Mark Display	Provision of solid-state surface barrier detectors and new video amplifier system to display alignment mark topography by back-scattered electron detection

Table 4.2
(Continued)

Problem	Solution or Modification
Coarseness of control	Provision of high-resolution, non-backlash rotating stage with ± 1° travel. Later replaced by rotationally rigid stage and electronic rotation by X/Y mixing.
Inadequate Pattern Scale Adjustment	Provision for fine trim potentiometers for X and Y scale
Non-Perpendicularity of X and Y Axes	Compensation by electrical cross-coupling of X and Y axes.
Lack of Adequate Astigmatism Control	Provision of calibrated potentiometers and stabilized supplies
Severe Instability in Electron Beam	Installation of additional electrostatic shields, design and fabrication of new stigmator with total electrostatic shields of insulating parts
Hysteresis in Precision Beam Positioning	Precision installation of high linearity air core deflection yokes
Limited Stage Travel	Modification of stage to give 1.25 x 1.0 inch travel
Word-Rate Dependent Data Errors	Addition of holding register to provide better read-write data control of core memory.

4.2 SOFTWARE FOR ELECTRON MICROPATTERN GENERATOR

A set of programs for writing and checking magnetic tapes containing EMG control information was developed. They are discussed individually below.

SEMTAPE/COMPILE

SEMTAPE/COMPILE is the name of the program employed for the major share of the reduction of artwork to EMG commands on magnetic tape. It also does the final conversion to tape instructions for discretionary metallization or interconnection patterns as specified by the assignment and routing programs discussed above under Section 3.2 The output from this program consists of 1) a magnetic tape for input to the EMG, and 2) a listing of the input cards followed by a block count (2048 bytes per block), and a reading of processor and input-output times, in seconds. There are four types of input card read by the program, namely parameter, rectangle, end-of-loop, and end-of-program:

1) Parameter card--contains program number, beamwidth, overlap, wordratecode, subscan code, x-origin, y-origin, x-step, y-step, x-repeat, y-repeat. These quantities are read with Burroughs B-5500 free-form format, but are restricted to a single card. The significance of these quantities is as follows (unless otherwise stated, quantities are zero if not set):
    a) program number--the last three digits (rounded integer) are emitted on the tape in BCD following a "set number register" command.

b) beamwidth--this expresses the effective exposure beam width in the grid scale unit of the problem. If beamwidth $\leq$ 1 or beamwidth $\geq$ 1023 an error message is printed and the program terminates. If not set, beamwidth = 2.

c) overlap--fraction of beamwith to be overlapped when stepping the beam address in order to assure reliable exposure. Must be between (not equal to) zero and one, or the program prints error message and terminates. If not set, overlap = .5.

d) wordratecode-emitted mod 16 as the argument of a "set word rate"command.

e) subscan code--emitted as the argument of a "set subscan" command (currently not implemented in this form).

f) x-origin, y-origin--provides the basis for translating the origin from the grid point 0,0.

g) x-step, y-step--for the step-repeat construct, specifies the step size in each direction of the dynamic origin.

h) x-repeat, y-repeat--for the step-repeat construct, specifies the number of replicates in each direction beyond the original version of the pattern. The program expects a parameter card (or alternatively a B-5500 control card which causes "normal" termination

of SEMTAPE/COMPILE) as the first data card, and as first card following card types 3 or 4 (end of loop, end of program). The present inadequate error checking may permit (invalid) continued processing of the data, but the results are, in general, useless.

2) Rectangle card--this is the device used to describe patterns for exposure. The data contained on it represent the initial x, initial y, width, final x, final y of a "line". Each of these quantities is accepted as an integer, right justified in a five column field, starting at columns 9, 14, 19, 24, and 29, respectively. The rest of the card is available for comments and identification. Addresses are interpreted relative to the dynamic origin of the step-repeat construct; if operating. The initial x must be non-negative (see card types 3 and 4). The program can only draw horizontal or vertical "lines", so in principle either the x or y coordinate remains unchanged from initial to final value. If this is not true of the values read, the average (initial and final) of that coordinate which changes less is used. If the dynamic absolute grid address leaves the range 0 to 4091 for x, or 0 to 4095 for y, a warning message will be printed and the nearest "in-bounds" address will be used. The ranges are unsymmetric at present since the x-address code for 1023 is a command flag. Zone changes, i.e., setting of new most-significant-bit (MSB) and next-most-significant-bit (NMSB) in the x- or y-address, are monitored and executed automatically.

3) End of loop card--this card delimits the end of a step-repeat pattern. Its format is identical to that of card type 2 (rectangle). It is distinguished by a negative initial x field and a non-negative initial y field; the remainder of the card is ignored. The program expects a parameter card following this card; alternatively, a B-5500 control card will terminate the program normally.

4) End of program card--this card marks the end of EMG programs (multiple programs may be written on a single tape in on run). It is essentially identical to card type 3, the only difference being the requirement for a negative initial y field as well as a negative initial x field. It can serve also to delimit a step-repeat loop, but when the loop is exhausted, a filled-out tape block will be forced, with an "end-of-program" command emitted as the last item. A temporary disk file is used to allow the step-repeat construct to retrieve pattern information (rectangles) which are repeated.

TEST/PATTERN

TEST/PATTERN is essentially an octal input translator for the EMG digital control. It has proved useful for generating tapes that exercise particular hardware features by supplying a repetitive octal pattern. Tapes maintain the standard blocking of 2048 bytes. Also outputted on the printer, is a listing of the input cards, followed by the size of the output tape in characters (bytes), feet written, and reading time at a tape unit speed of 36 inches per second; then the

B-5500 processor and I-O times are printed. There are two input entries. The sampler is just the number of copies of the original pattern to be written on the tape. This is entered with the B-5500 control card construct,

?CØMMØN = n.

The other item is the card file describing the octal pattern. Columns 1-64 of the card are used; the remainder may be used for identification. The data columns are assumed to contain octal digits (0,1,...,7); if any other character is encountered the low order 3 bits of its internal code (BCL) will be used as an octal digit. The program detects the last card, which is treated slightly differently: from column 65 (or the first blank column, or any character whose internal code (BCL) has a first bit of one) on, the data is ignored. Patterns extending up to 1500 cards (96,000 octal digits) can be accommodated.

SEMTAPE/LISTER

SEMTAPE/LISTER is a program used to check the contents of a magnetic tape made for the EMG. It lists the block number and relative record (4 bytes) within a block, the octal contents of the record, the interpretation of the contents as a command or beam address instruction, and simulation of the contents of the EMG digital control registers and state of the EMG. Presently, the interpretation and simulation portions correspond to the original version of the EMG which used only a 1024 x 1024 position address raster. Adaptation to the present version has been deferred since the program is still usable in this form for machine trouble-shooting purposes.

SIMSEM/CALCØMP

SIMSEM/CALCØMP is another checking program which translates an EMG tape into a Calcomp tape. The various EMG programs on the tape are plotted as 10-inch frames with the program number at the side and the time and date of generation of the Calcomp tape at the end of the plot. Printer output consists of a list of the block-addresses on the EMG tape at which "end-of-program" commands occur, and the B-5500 processor and I-O times. This program has not been adapted to the larger 4092 x 4096 position address grid because the resolution available on the Calcomp is only 1/1500 of the 10-inch full scale. Furthermore, the conversion and plotting process have proven to be rather slow.

5.0 DISCUSSION

The work performed under this program has resulted not only in the tools and methods for interconnecting in a meaningful way a random arrangement of tested viable circuit elements or modules, but has also given support to the further development of the high-quality digitally-controlled electron beam pattern generator, the Electron Micropattern Generator, which can presently expose pattern geometries in an electron sensitive resist with elements as small as one micron and which can yield $\pm$ 1/2 micron or better alignment accuracies of a pattern exposure with pre-existing fiducial marks on the substrate. The failure of the program to yield operating circuits was due only to the exhaustion of the support available; the most recent improvements on the tools and methods, made in the last few months, have brought these procedures to a level of high utility. The question of adhesion of the final metallization is a minor problem which almost certainly can be solved by the use of sputter etching immediately prior to metal deposition. The trial device patterns, for the 4 x 4 gate array, were perfected, and the custom interconnection software was completely debugged so as to yield solutions which properly matched the gate array geometry. Nothing, therefore, would prevent the realization of working circuits of the present or similar design, using these techniques, if given the required small additional effort.

5.1 FUTURE DIRECTIONS

The manufacture of integrated circuits with the help of electron beam lithography for defining device and circuit patterns opens the door to fabrication of entire electronic systems on a single block

or chip of silicon, by virtue of the high density of components and circuits which this technique allows. For instance, memory cell areas as small as 1.2×10^{-6} cm^2 and gate areas down to 4×10^{-6} cm^2, which are achievable with electron beam lithography, will permit fabrication of an entire electron system such as a 20,000-gate 256,000-bit memory computer on a 1 cm^2 chip. The problems requiring solution in order to achieve this goal of ultra-large-scale-integration (ULSI) range beyond electron-beam lithography aspects and also include, as shown in Figure 5.1, high density processing, defect accommodation, device design, system design and layout, testing, and packaging. Particularly important are defect accommodation techniques, because planar technology at present and for the near future offers no hope of obtaining a defect-free complex device or system on a chip as large as 1 cm^2.

The overall concept of defect accommodation technique is shown in Figure 5.2. Using present electron beam fabrication methods, a group of high-density integrated circuit modules are fabricated on a large chip and internally connected so as to be operational. Defect accommodation technique consists of testing for good or bad modules and then wiring around the bad modules by a computer-derived lead routing pattern applied to the final metallization. Because the electron beam can be used for the electrical testing of the modules at very high speed, as well as for drawing the final metal patterns, also at very high speed, the defect accommodation may be accomplished in an on-line economic manner.

Dwg. 2926A56

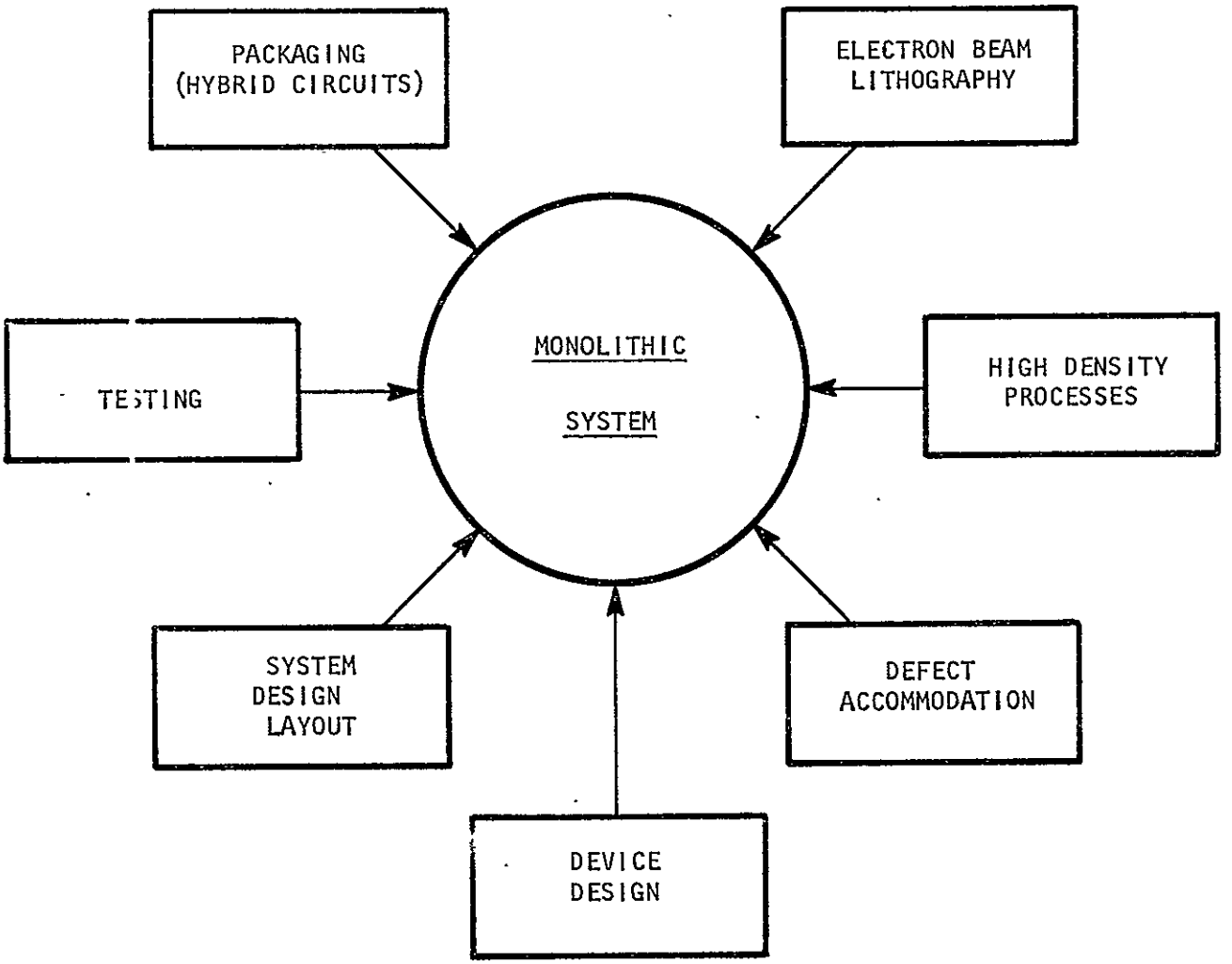


Figure 5.1 Ultra large scale integration (ULSI)

Dwg. 2926A57

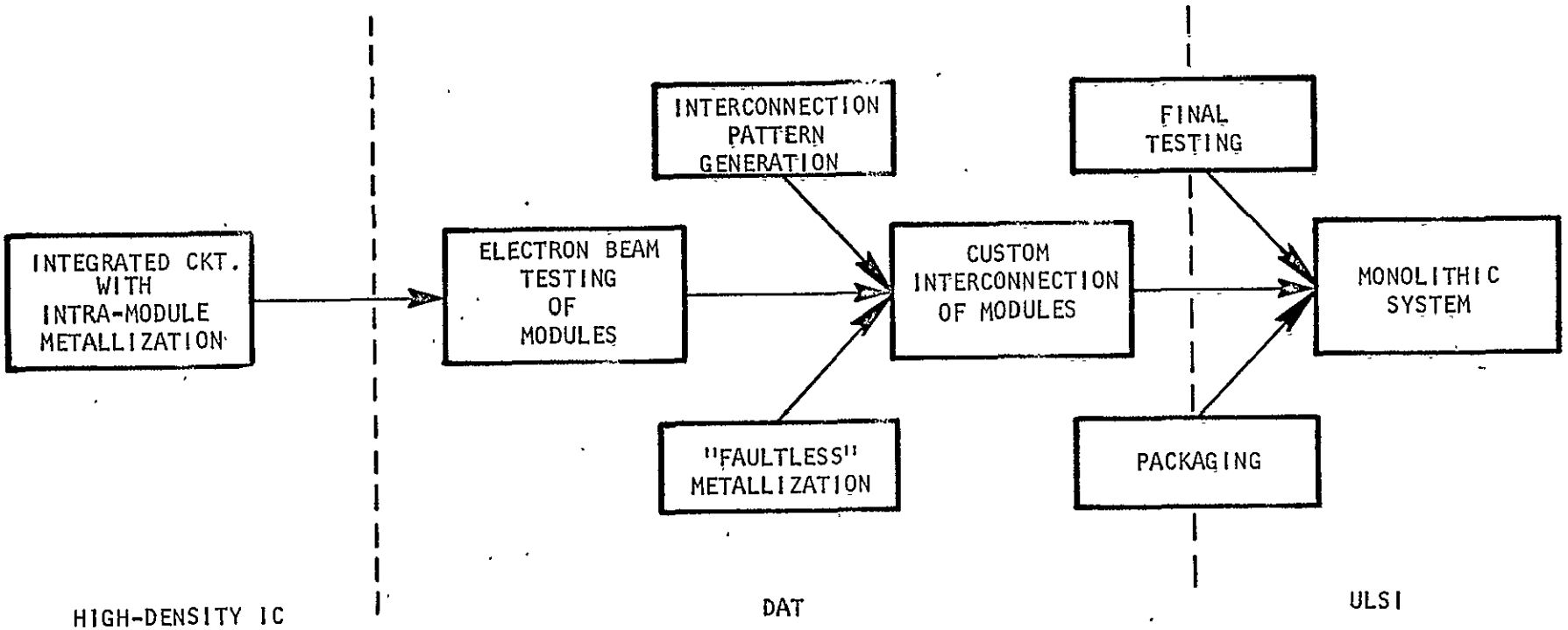


Figure 5.2 Defect accommodation technique (DAT)

The smallest area of metal that can be contacted satisfactorily with a mechanical fine wire probe system is about 75 x 75 microns (which is larger than individual logic gates in high density circuits), while an electron beam can be accurately addressed to an area as small a 1 x 1 micron. The electron beam can be used both as input probe and output probe. The chief difficulty with its use is that it can only be used as a single beam, and some means is required for holding input signals at desirable levels as set by the beam while the beam goes to other addresses or locations to set other input conditions or to probe the circuit output conditions. Therefore it is important to develop effective techniques 1) for permitting a single electron beam to set up test conditions for a circuit, 2) for accurately measuring circuit parameters such as output voltages by a single electron beam probe, and 3) for performing the testing and executing the appropriate discretionary wiring pattern in a single, on-line process. When these techniques are mastered, the defect accommodation technique will be effective, making possible the realization of very complex circuitry on a silicon monolith.